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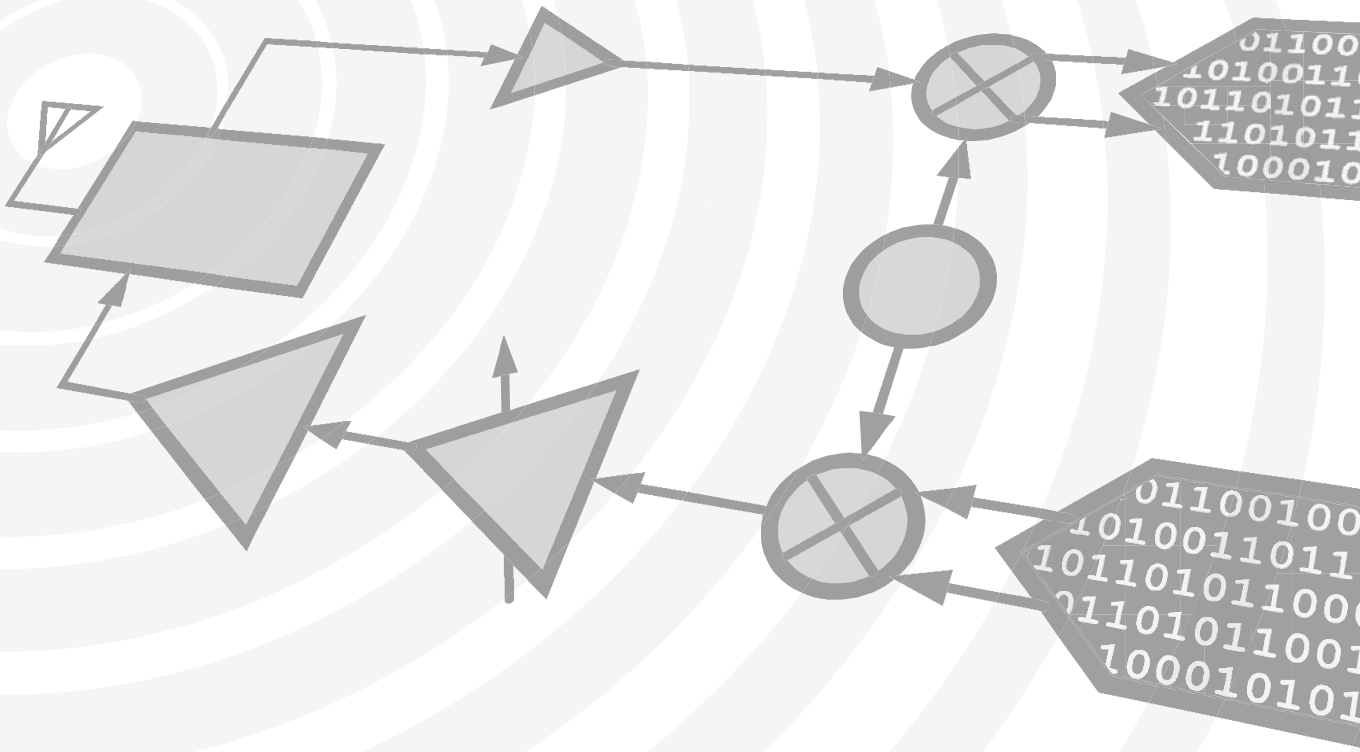
NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED



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v02.0113

HMC1090LP3E

BROADBAND HIGH IP3 DOWNCONVERTER 0.7 - 3.5 GHz

Typical Applications

The HMC1090LP3E is ideal for:

- Multiband/Multi-standard Cellular BTS Diversity Receivers
- GSM & 3G & LTE/WiMAX/4G
- MIMO Infrastructure Receivers
- Wideband Radio Receivers
- Multiband Basestations & Repeaters

Features

Broadband Operation with no external matching

High-side and Low-side LO injection Operation

Wide IF Frequency Range

High Input IP3 of +25 dBm

Power Conversion Gain of 7.9 dB

Input P1dB of 12 dBm

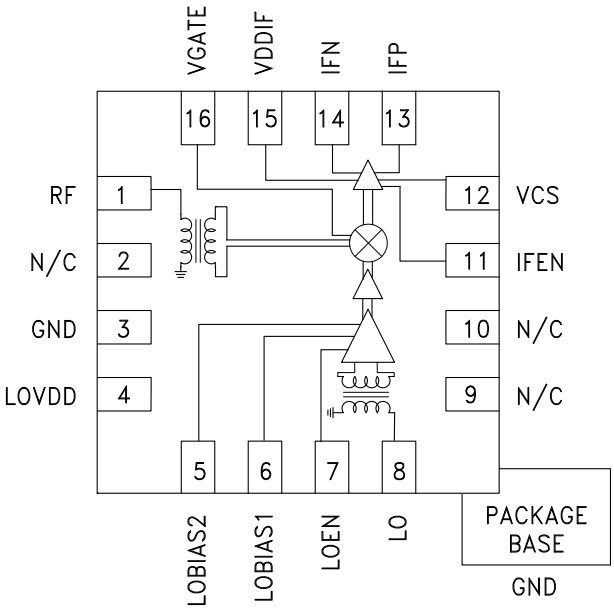
SSB Noise Figure of 10 dB

Dedicated Enable Pins for IF & LO amplifiers

Single-ended RF & LO input ports

Compact Solution, 3x3 mm QFN Package

Functional Diagram



General Description

The HMC1090LP3E is a high linearity, single channel downconverting mixer optimized for multi-standard diversity receiver applications that require low power consumption and small size. The HMC1090LP3E features new wideband limiting LO amplifiers to achieve an unprecedented RF bandwidth of 700 MHz to 3500 MHz. Unlike conventional narrow-band down-converter RFICs, the HMC1090LP3E supports both high-side and low-side LO injection over the entire RF frequency band. The RF and LO input ports are internally matched to 50Ω.

The HMC1090LP3E integrates LO and IF amplifiers with enable functions, LO and RF baluns and high linearity passive mixer cores with bias control interface. The balanced passive mixer combined with the high-linearity IF amplifier architecture provides excellent LO-to-RF, LO-to-IF and RF-to-IF isolations. The HMC1090LP3E provides a very low noise figure of 10 dB, and high IIP3 of +25 dBm allowing the device to be used in demanding wideband applications. The HMC1090LP3E's input IP3 can be further improved by external matching in narrow-band applications. The HMC1090LP3E exhibits less than 1.5W power consumption which can be optimized through external bias control pins. The HMC1090LP3E also features a very fast enable control interface for reduced power consumption in Time Division Duplex (TDD) applications. The HMC1090LP3E is housed in a RoHS compliant 3x3 mm leadless QFN package.

BROADBAND HIGH IP3 DOWNCONVERTER 0.7 - 3.5 GHz

Electrical Specifications, T_A = +25°C, IF Frequency = 150 MHz, LO Power = 0 dBm, RF Input Power = -5 dBm, LOVDD = 3.3V, VCS=VBIAS_IF[3]=VDDIF = 5V

Parameter	Typ.	Typ.	Typ.	Typ.	Units
RF Frequency	900 [1]	1900 [2]	2200 [2]	2700 [2]	MHz
Conversion Gain [8]	8.4	8.3	8.2	7.3	dB
IP3 (Input)	25.8	24.6	24.2	25.1	dBm
Noise Figure (SSB)	8.5	9.4	9.7	10.5	dB
1 dB Compression (Input)	10.7	12.4	12.5	13.0	dBm
LO leakage @ RF port	-64	-55	-55	-61	dBm
RF to IF Isolation	41	37	37	38	dB
+2RF-2LO Response	68	65	62	65	dBc
+3RF-3LO Response	64	85	82	83	dBc
LO Input Drive Level	-3 to +3	-3 to +3	-3 to +3	-3 to +3	dBm

DC Power Supply Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units.
IF Supply Voltage (VBIAS_IF[3], VDDIF[4])		+4.75	+5	+5.25	V
LO Supply Volltage (LOVDD)		+3.15	+3.3	+3.45	V
IF Amplifier Supply Current when enabled	VDDIF[3]		91		mA
	VBIAS_IF[4]		15		mA
	VCS[5]		2		mA
IF Amplifier Supply Current when disabled	VDDIF[3]		0		mA
	VBIAS_IF[4]		1.6		mA
	VCS[5]		2.7		mA
LO Amplifier Supply Current when enabled	LOVDD		114		mA
	LOBIAS1[6] + LOBIAS2[6]		4.5		mA
LO Amplifier Supply Current when disabled	LOVDD		2.7		mA
	LOBIAS1[6] + LOBIAS2[6]		5.2		mA

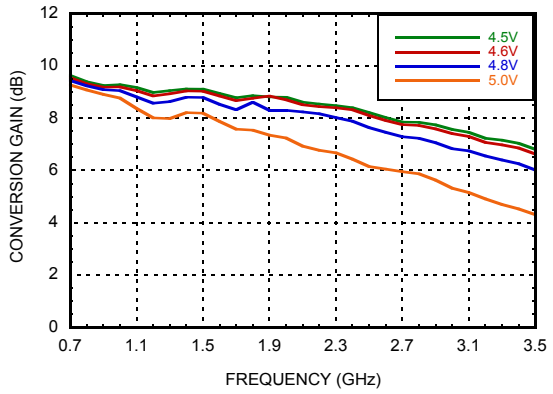
LO/IF, Enable/Disable Interface Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units.
LOEN High Level	LO Amplifier Disabled	+3	+5		V
LOEN Low Level	LO Amplifier Enabled	0	0	+1	V
IFEN High Level	IF Amplifier Disabled	+3	+5	5	V
IFEN Low Level	IF Amplifier Enabled	0	0	+1	V
Enable Settling Time[7]			30		ns
Disable Settling Time[7]			30		ns

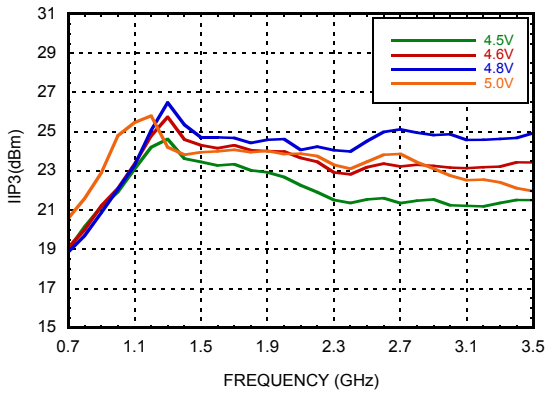
[1] High side LO injection, VGATE = 5.0V [2] Low side LO injection, VGATE = 4.8V
[3] Supply voltage for IF amplifier through choke inductor. See application circuit.
[4] Supply voltage for bias circuit of IF amplifier. See application circuit.
[5] Bias Control pin for IF amplifier. See application circuit.
[6] Bias Control pins for LO amplifier. See application circuit.
[7] Remove bypass capacitors on LOEN and IFEN pins for given settling times. See application circuit.
[8] Balun losses at IF output ports are de-embedded.

BROADBAND HIGH IP3 DOWNCONVERTER 0.7 - 3.5 GHz

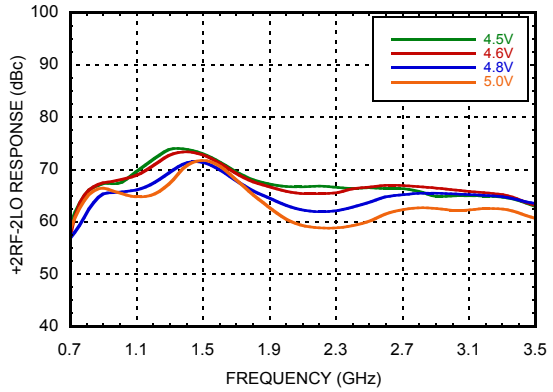
Conversion Gain vs. VGATE[1]



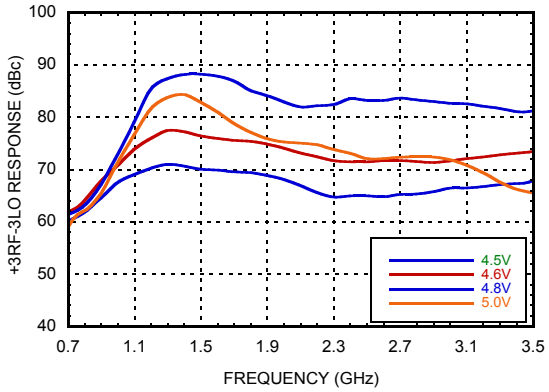
Input IP3 vs. VGATE[1]



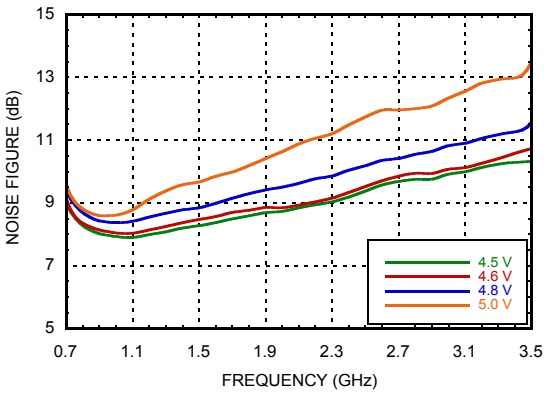
+2RF -2LO Response vs. VGATE[1]



+3RF -3LO Response vs. VGATE[1]

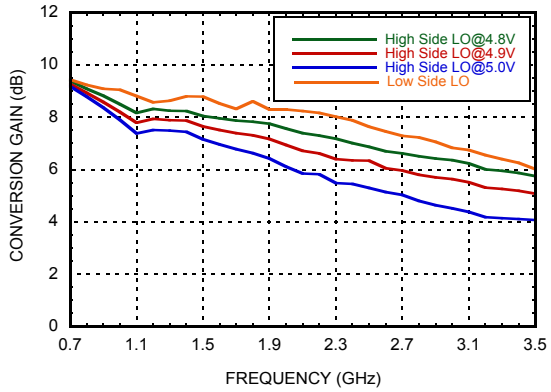


Noise Figure vs. VGATE[1]

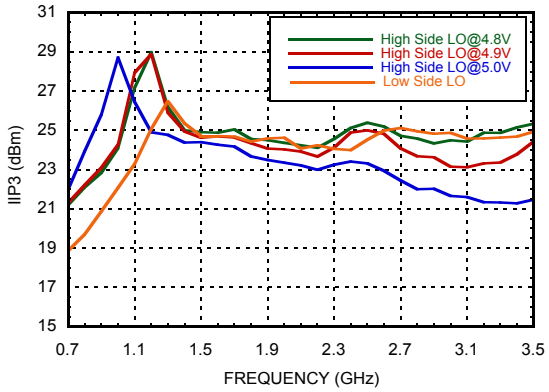


[1] VGATE is bias voltage for passive mixer cores. Refer to pin description table.
Balun losses at IF output ports are de-embedded.

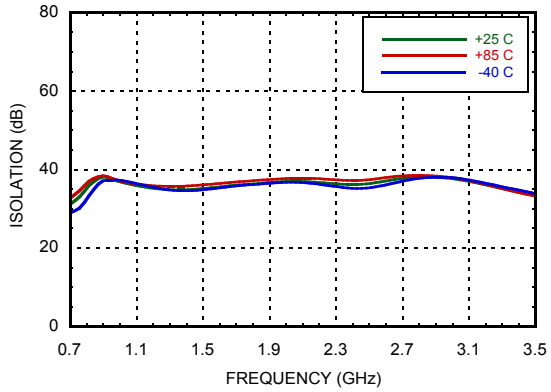
Conversion Gain vs. High Side LO & Low Side LO @ VGATE = 4.8V



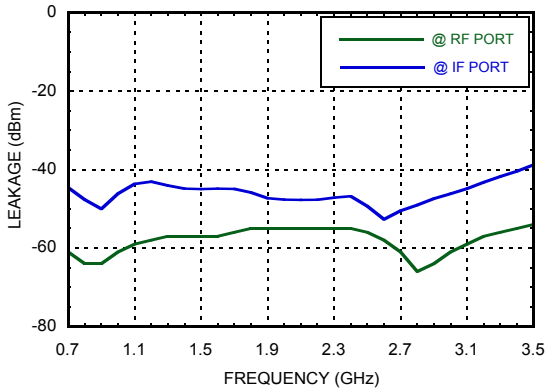
Input IP3 vs. High Side LO & Low Side LO @ VGATE = 4.8V



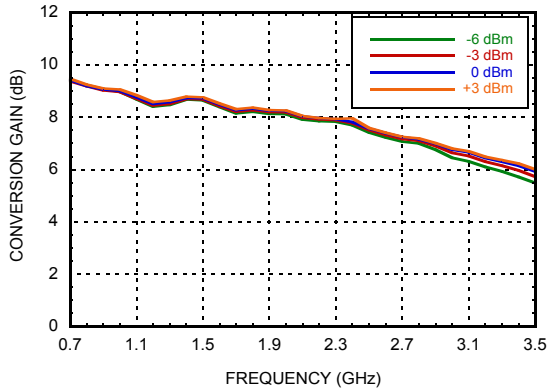
RF/IF Isolation vs. Temperature @ VGATE = 4.8V



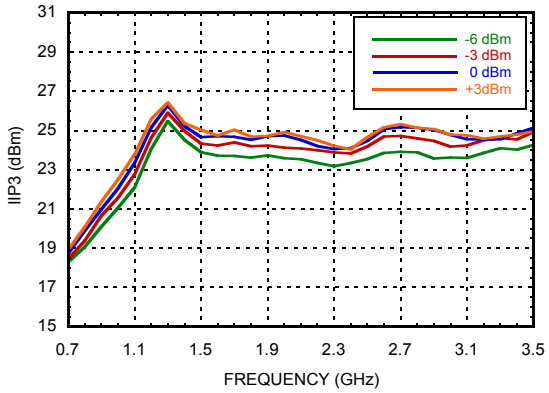
LO Leakage @ VGATE = 4.8V



Conversion Gain vs. LO Drive @ VGATE = 4.8V



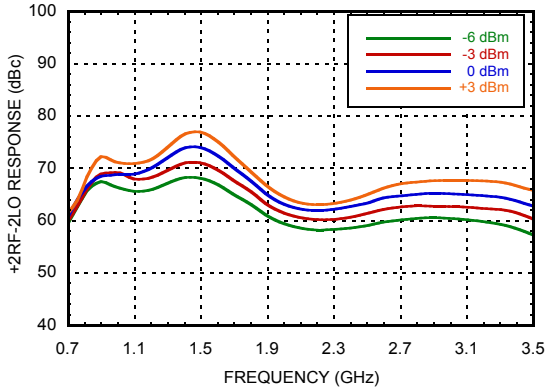
Input IP3 vs. LO Drive @ VGATE = 4.8V



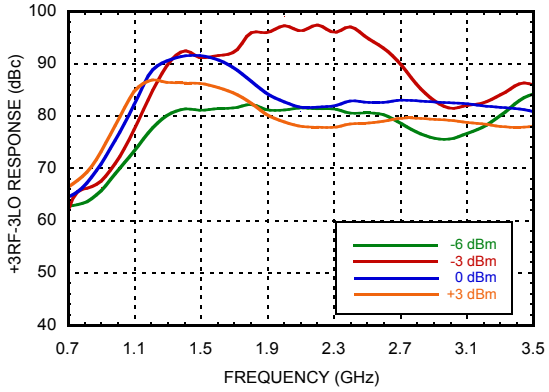
Balun losses at IF output ports are de-embedded.

BROADBAND HIGH IP3 DOWNCONVERTER 0.7 - 3.5 GHz

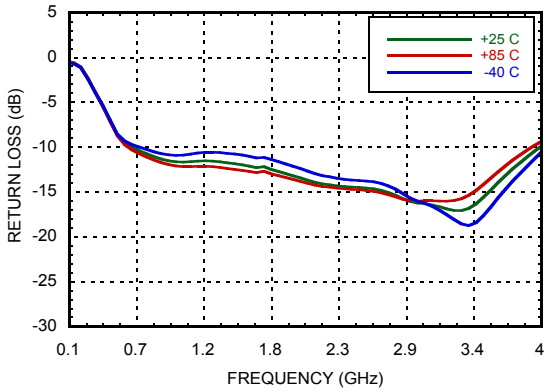
+2RF, -2LO Response vs. LO Drive @ VGATE = 4.8V



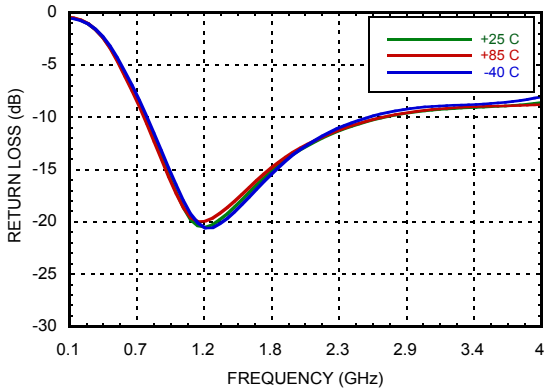
+3RF, -3LO Response vs. LO Drive @ VGATE = 4.8V



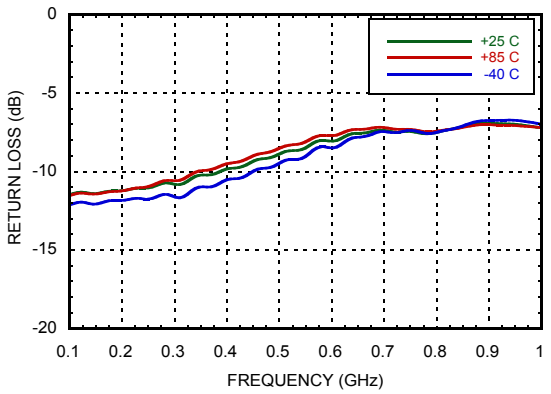
RF Input Return Loss @ VGATE = 4.8V [1]



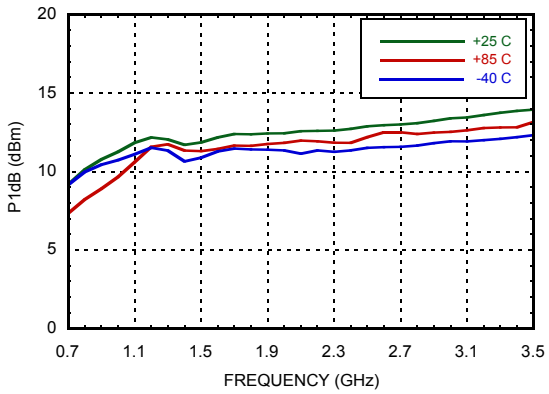
LO Input Return Loss @ VGATE = 4.8V



IF Output Return Loss @ VGATE = 4.8V [1]



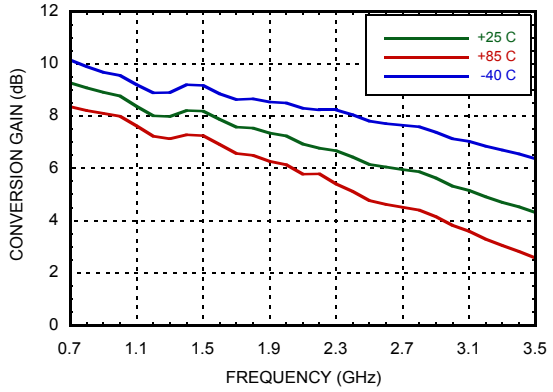
Input P1dB vs. Temperature @ VGATE = 4.8V



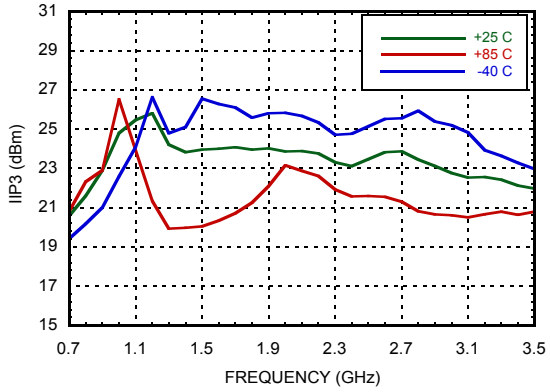
[1] LO input Frequency = 1500MHz, LO power = 0 dBm.

BROADBAND HIGH IP3 DOWNCONVERTER 0.7 - 3.5 GHz

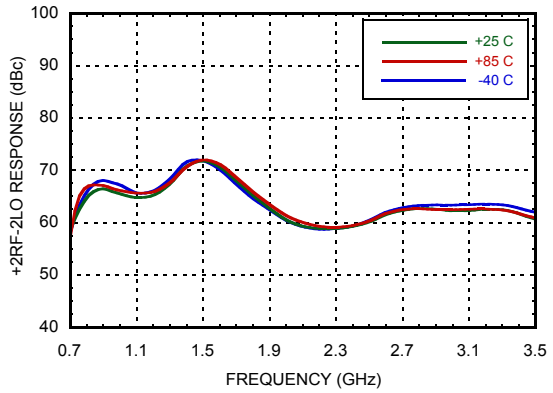
Conversion Gain vs. Temperature @ VGATE = 5.0V



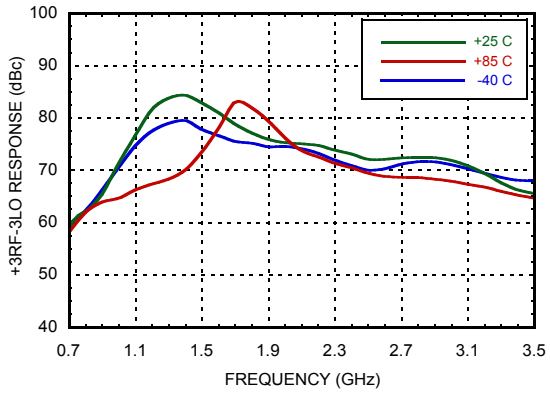
Input IP3 vs. Temperature @ VGATE = 5.0V



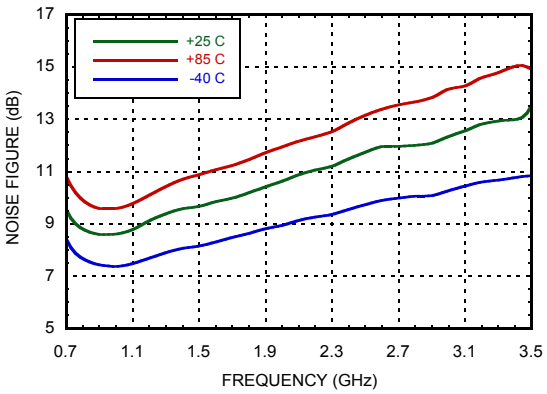
+2RF, -2LO Response vs. Temperature @ VGATE = 5.0V



+3RF, -3LO Response vs. Temperature @ VGATE = 5.0V



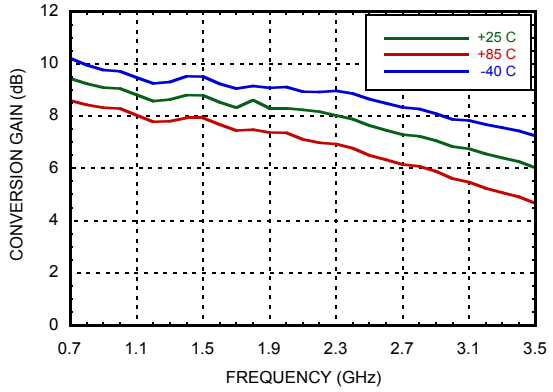
Noise Figure vs. Temperature @ VGATE = 5.0V



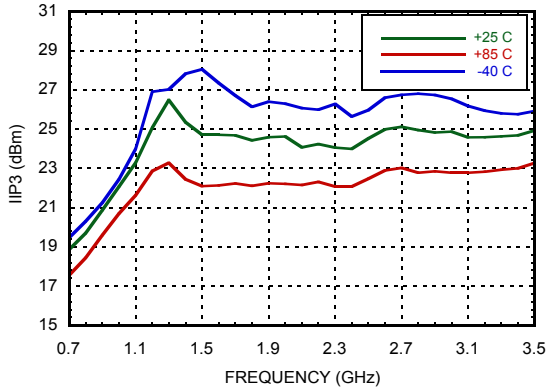
Balun losses at IF output ports are de-embedded.

BROADBAND HIGH IP3 DOWNCONVERTER 0.7 - 3.5 GHz

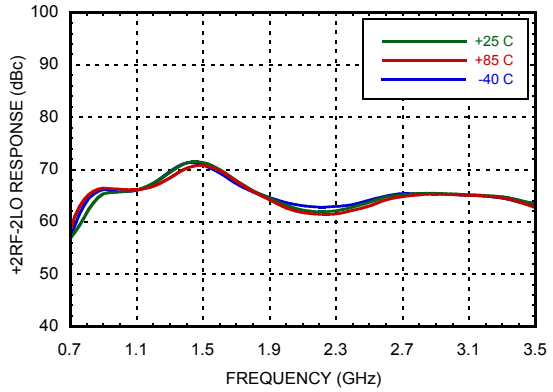
Conversion Gain vs. Temperature @ VGATE = 4.8V



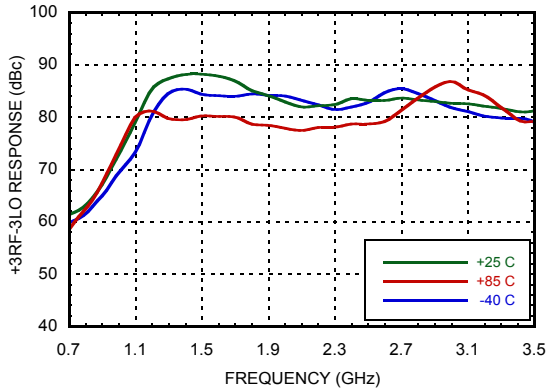
Input IP3 vs. Temperature @ VGATE = 4.8V



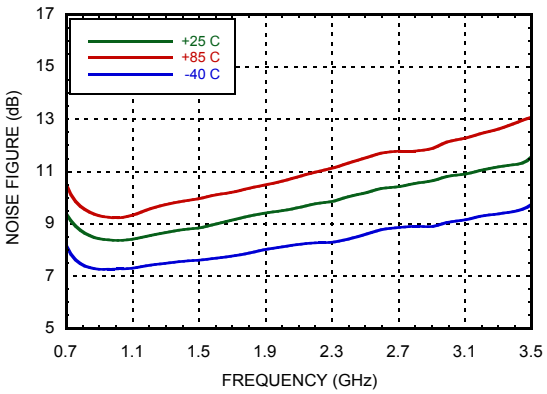
+2RF, -2LO Response vs. Temperature @ VGATE = 4.8V



+3RF, -3LO Response vs. Temperature @ VGATE = 4.8V



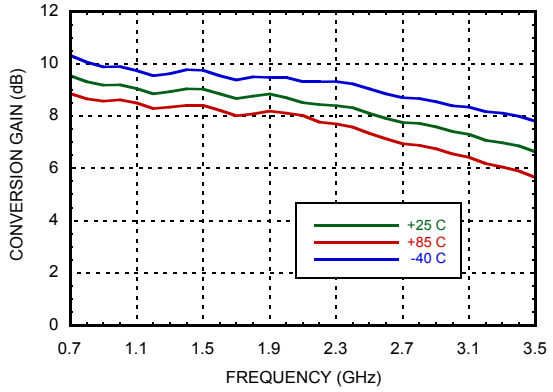
Noise Figure vs. Temperature @ VGATE = 4.8V



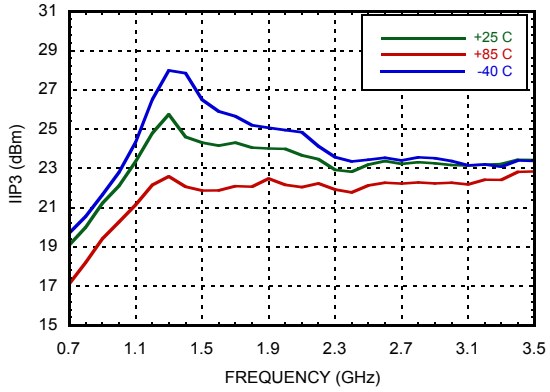
Balun losses at IF output ports are de-embedded.

BROADBAND HIGH IP3 DOWNCONVERTER 0.7 - 3.5 GHz

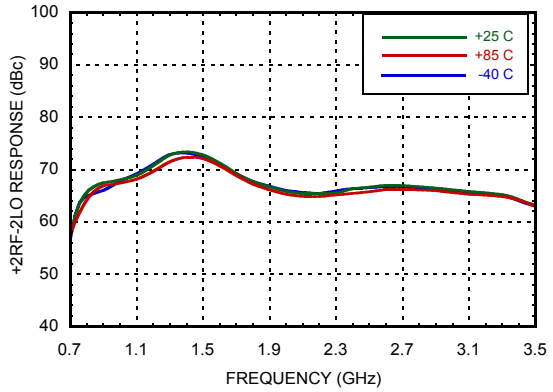
Conversion Gain vs. Temperature @ VGATE = 4.6V



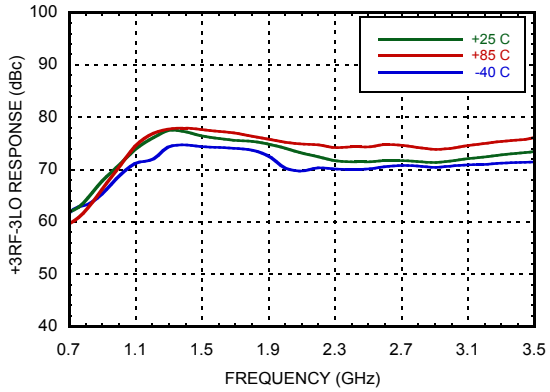
Input IP3 vs. Temperature @ VGATE = 4.6V



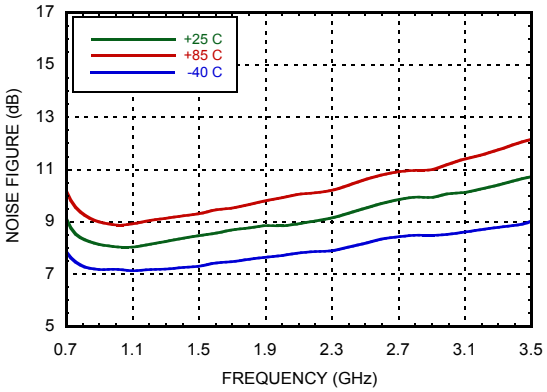
+2RF, -2LO Response vs. Temperature @ VGATE = 4.6V



+3RF, -3LO Response vs. Temperature @ VGATE = 4.6V

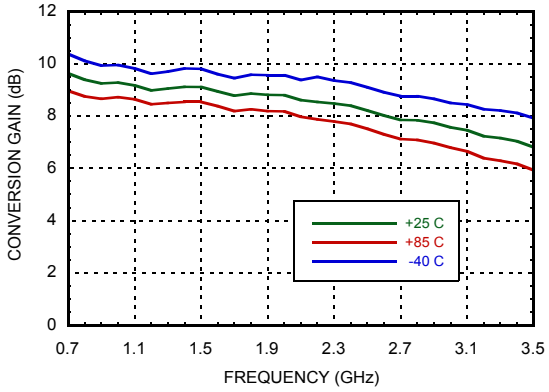


Noise Figure vs. Temperature @ VGATE = 4.6V

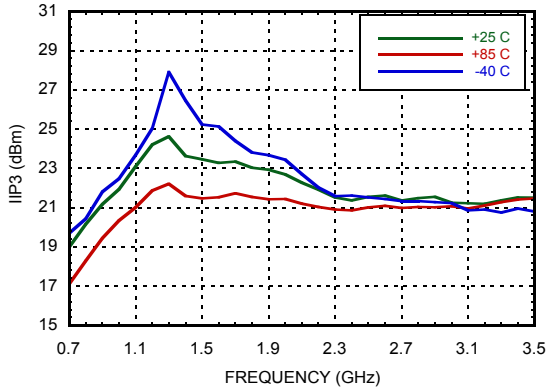


Balun losses at IF output ports are de-embedded.

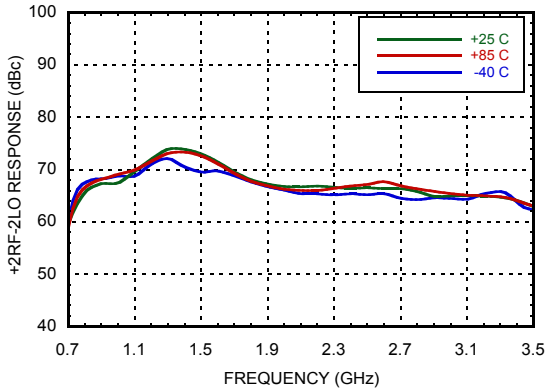
Conversion Gain vs. Temperature @ VGATE = 4.5V



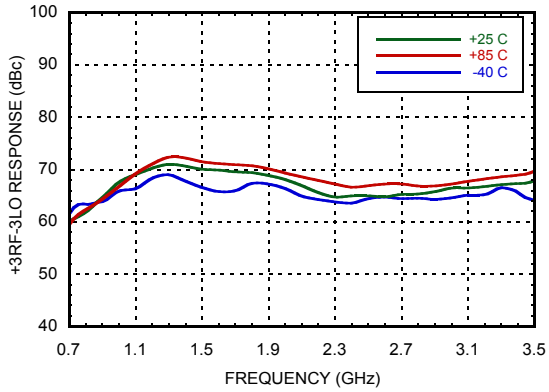
Input IP3 vs. Temperature @ VGATE = 4.5V



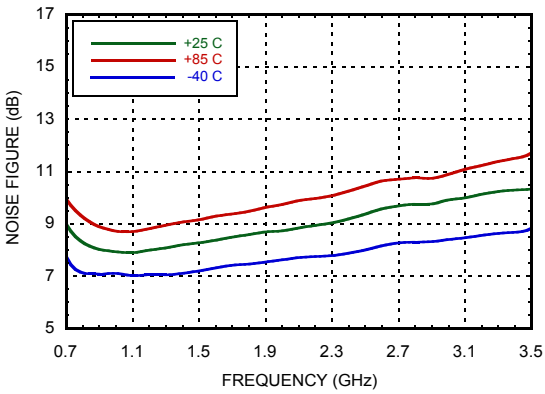
+2RF, -2LO Response vs. Temperature @ VGATE=4.5V



+3RF, -3LO Response vs. Temperature @ VGATE=4.5V



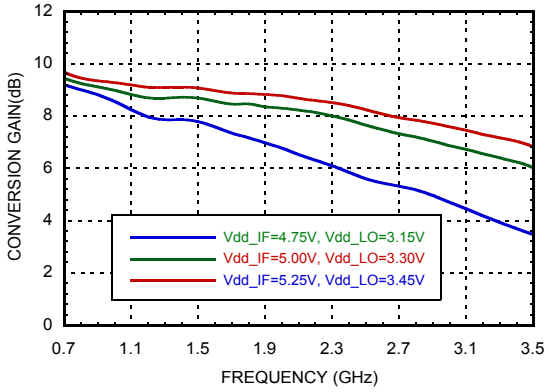
Noise Figure vs. Temperature @ VGATE = 4.5V



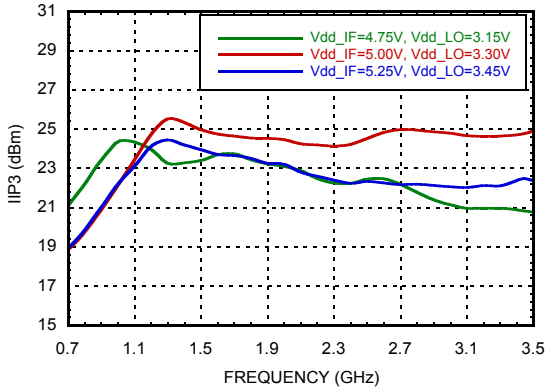
Balun losses at IF output ports are de-embedded.

BROADBAND HIGH IP3 DOWNCONVERTER 0.7 - 3.5 GHz

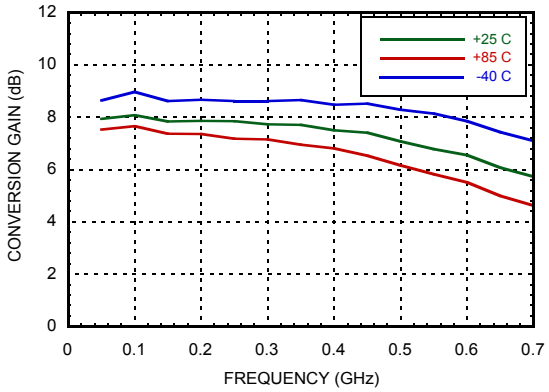
Conversion Gain vs. Vdd @ VGATE = 4.8V



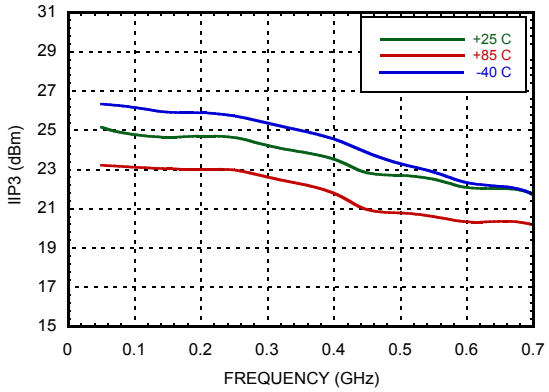
Input IP3 vs. Vdd @ VGATE = 4.8V



Conversion Gain vs. IF Frequency @ LO=1800 MHz, VGATE = 4.8V



IIP3 vs. IF Frequency @ LO=1800 MHz, VGATE = 4.8V



Balun losses at IF output ports are de-embedded.

BROADBAND HIGH IP3 DOWNCONVERTER 0.7 - 3.5 GHz

Harmonics of LO

	nLO Spur @ RF Port			
LO Freq. (GHz)	1	2	3	4
0.7	-55	-48	-68	-57
1.1	-53	-50	-66	-58
1.5	-51	-49	-66	-49
1.9	-48	-49	-60	-48
2.3	-49	-51	-56	-53
2.7	-55	-45	-52	-46
3.1	-51	-44	-55	-36
3.5	-47	-44	-52	-30

LO = 0 dBm
All values in dBm measured at RF port.

MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xx	-52	-24	-61	-36
1	-50	0	-43	-24	-59
2	-52	-56	-74	-54	-67
3	-85	-74	-67	-55	-75
4	-70	-38	-59	-24	-43

RF Freq. = 0.9 GHz @-5 dBm
LO Freq. = 0.75 GHz @ 0 dBm
All values in dBc below IF power level (1RF - 1LO).

MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xx	-49	-27	-64	-45
1	-44	0	-57	-46	-70
2	-58	-68	-64	-75	-76
3	-110	-88	-102	-93	-105
4	-108	-109	-110	-110	-110

RF Freq. = 1.9 GHz @-5 dBm
LO Freq. = 1.75 GHz @ 0 dBm
All values in dBc below IF power level (1RF - 1LO).

MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xx	-50	-39	-56	-44
1	-43	0	-53	-47	-76
2	-79	-69	-62	-76	-82
3	-107	-88	-108	-97	-109
4	-109	-107	-110	-110	-108

RF Freq. = 2.5 GHz @-5 dBm
LO Freq. = 2.35 GHz @ 0 dBm
All values in dBc below IF power level (1RF - 1LO).

Typical Supply Current vs. Vdd

VDDIF (V)	Idd_IF (mA)	LOVDD (V)	Idd_LO (mA)
4.75	110	3.15	113
5.00	112	3.30	114
5.25	112	3.45	115

Truth Table

IFEN (V)	IFAMP	LOEN (V)	LO_STAGES
Low	ON	Low	ON
High	OFF	High	OFF

BROADBAND HIGH IP3 DOWNCONVERTER 0.7 - 3.5 GHz

Absolute Maximum Ratings

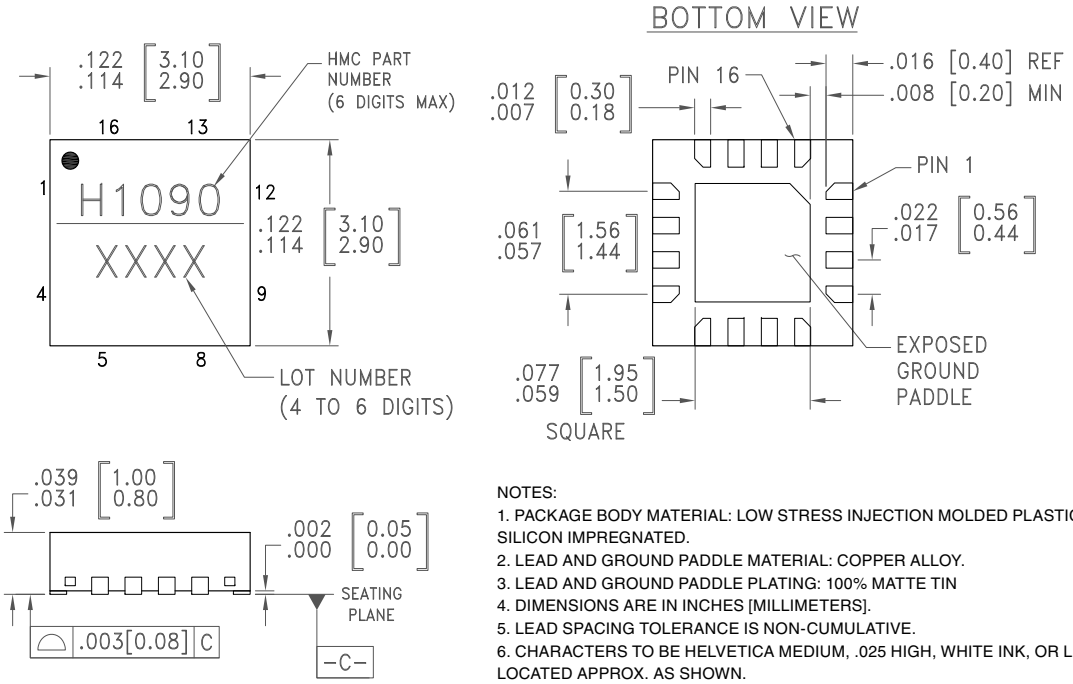
RF Input Power (VDDIF= +5V, LOVDD=3.3V)	+20 dBm
LO Input Power (VDDIF= +5V, LOVDD=3.3V)	+20 dBm
VDDIF, LOVDD	6V
VGATE	5.5V
Max. Channel Temperature	175°C
Continuous Pdiss (T = 85°C) (derate 41.8 mW/°C above 85°C)	2.72 W
Thermal Resistance (channel to ground paddle)	23.9 °C/W
Storage Temperature	-65 to 150°C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1B

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Junction Temperature			150	°C
Ambient Temperature	-40		85	

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



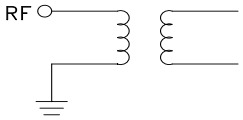
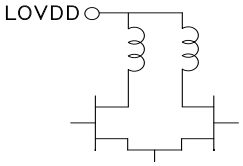
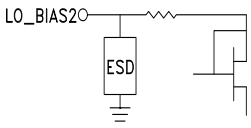
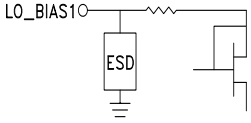
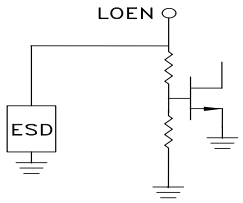
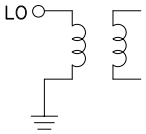
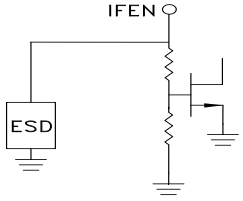
NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

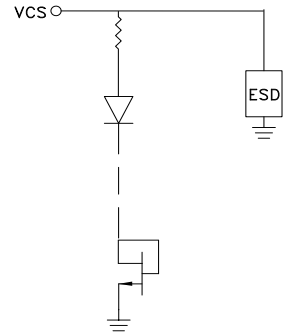
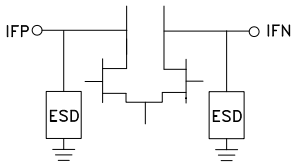
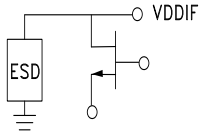
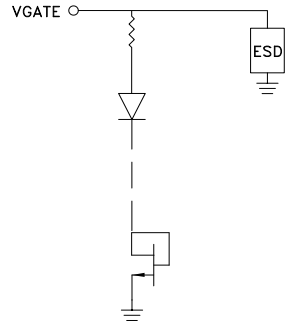
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking
HMC1090LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	H1090 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

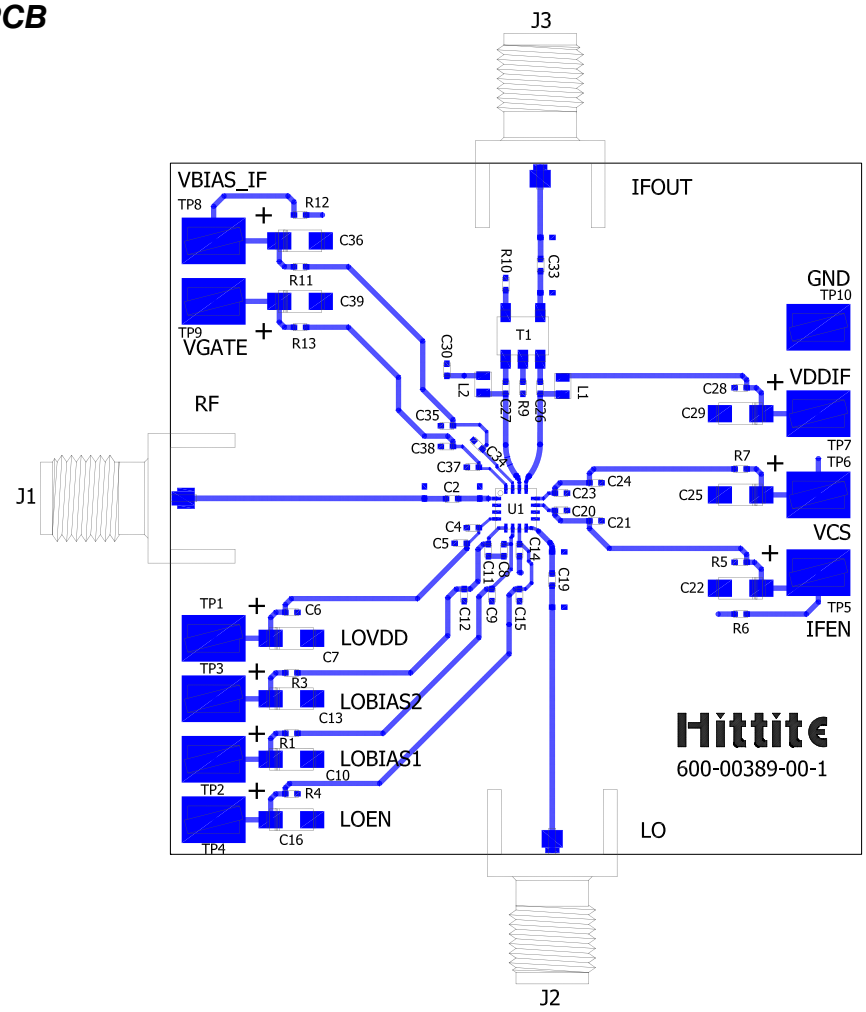
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	RF	RF input pin of the mixer, internally matched to 50 Ohms. The RF input pin requires off-chip DC blocking capacitors. See application circuit.	
2,9,10	N/C	Not connected internally.	
3	GND	This pin and the package base must be connected to RF and DC ground.	
4	LOVDD	3.3V bias supply for LO Drive stages. Refer to application circuit for appropriate filtering.	
5	LO_BIAS2	Bias control pin for LO Amplifier. Connect to 5V supply through 390 Ohms resistor. Refer to application section for proper values of resistors to adjust LO amplifier current.	
6	LO_BIAS1	Bias control pin for LO Amplifier. Connect to 5V supply through 270 Ohms resistor. Refer to application section for proper values of resistors to adjust LO amplifier current.	
7	LOEN	Enable for LO Amplifier. When connected to LOW or left unconnected, amplifiers are enabled. For disable mode connect to HIGH.	
8	LO	LO input of the mixer. Internally matched to 50 Ohms. Requires off-chip DC blocking capacitor. See application circuit.	
11	IFEN	Enable for IF Amplifier. When connected to LOW or left unconnected, amplifier is enabled. For disable mode connect to HIGH.	

Pin Descriptions *(continued)*

Pin Number	Function	Description	Interface Schematic
12	VCS	Bias control pin for IF amplifier. Connect to 5V supply through 240 Ohms resistor. Refer to application section for proper values of resistors to adjust IF amplifier current.	
13,14	IFP, IFN	Differential IF outputs.Connect to 5V supply through choke inductors. See application circuit.	
15	VDDIF	Supply voltage pin for IF amplifier's bias circuits. Connect to 5V supply through filtering.	
16	VGATE	Bias pins for mixer cores. Set from 4.4V to 5.0V for operating frequency band.	

Evaluation PCB



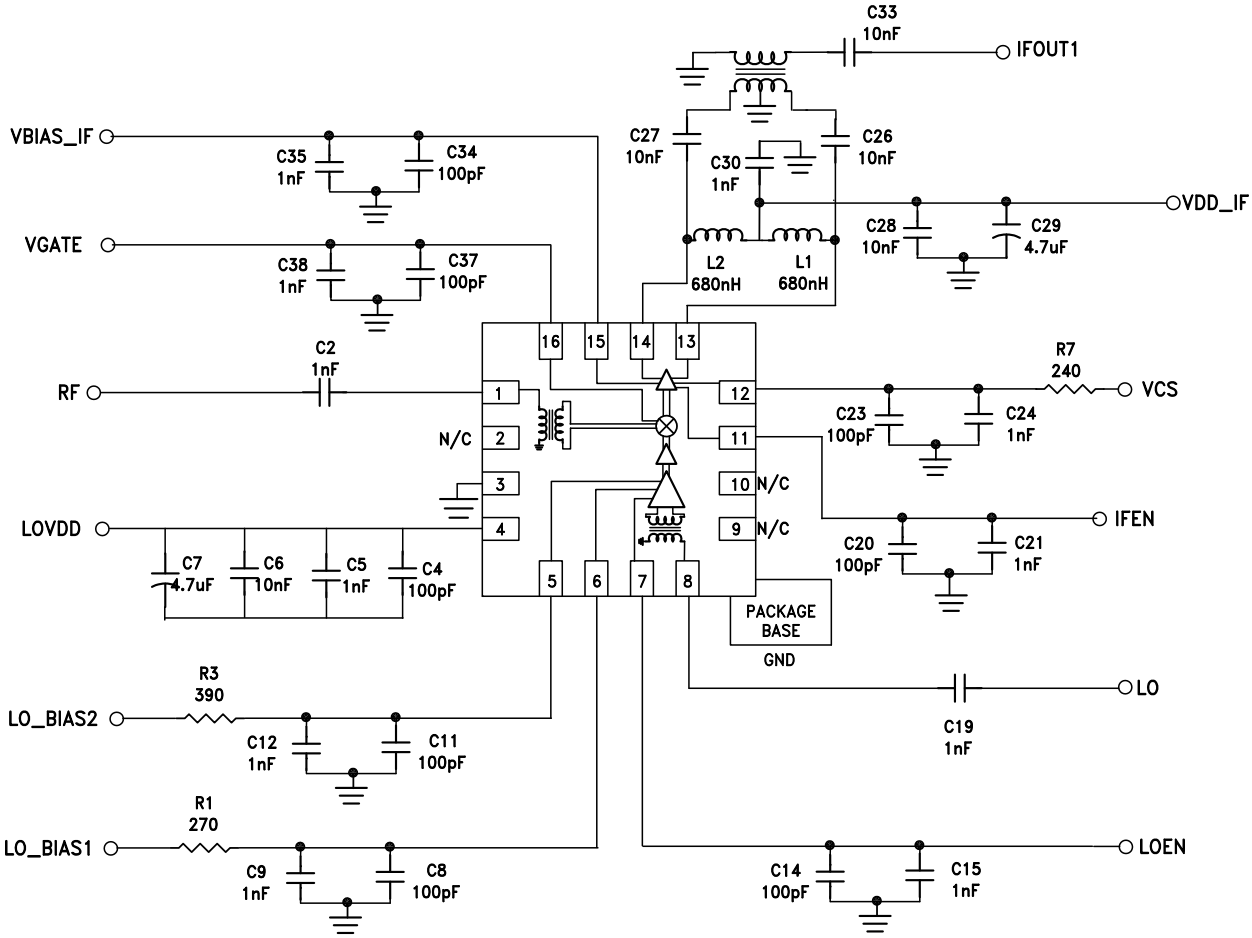
List of Materials for EVAL01- HMC1090LP3E [1]

Item	Description
J1 - J3	PCB Mount SMA Connector
TP1-TP10	Test Point
L1-L2	680 nH Inductor, 0603 Pkg.
C26-28, C33	0.01 µF Capacitor, 0603 Pkg
C7,C10,C13,C16,C22,C25,C29,C36,C39	4.7 µF CaSE A, Tantalum
C4,C8,C11,C14,C20,C23,C34,C37	100 pF Capacitor, 0402 Pkg.
C2,C5,C9,C12,C15,C19,C21,C24,C30,C35,C38	1 nF Capacitor, 0402 Pkg.
C6	10 nF Capacitor, 0402 Pkg.
R4-R6,R9-R13	0 ohm Resistor, 0402 Pkg.
R1	270 ohm Resistor, 0402 Pkg.
R3	390 ohm Resistor, 0402 Pkg.
R7	240 Ohm Resistor, 0402 Pkg.
T1	1:4 Transformer - ETC4-1T-7TR.

[1] Reference this number when ordering complete evaluation PCB

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit - Broadband



Notes:

1-Differential IF output transmission lines should be symmetrical

2-Refer to evaluation PCB for component placements and distances

Application Information

The HMC1090LP3E is a broadband single channel, high dynamic range, high gain, low noise, high-linearity down-converting mixer designed for RF frequencies from 700 MHz to 3.5 GHz. The HMC1090LP3E's low noise and high linearity performance makes it suitable for a wide range of transmission standards, including TDD, FDD, LTE, CDMA, GSM, MC-GSM, W-CDMA, UMTS, TD-SCDMA and WiMAX applications.

The HMC1090LP3E offers an easy-to-use and complete frequency conversion solution for broadband receiver applications in a highly compact 3x3 mm QFN package. The HMC1090LP3E greatly simplifies the design of receiver applications by increasing the integration level and reducing the number of required circuit elements thereby reducing cost, area, and power consumption.

Principle of Operation

The HMC1090LP3E incorporates a double-balanced passive mixer which is driven from a single-ended LO input that is broadband matched to 50 Ω and requires only a standard DC-blocking capacitor. The single-ended LO input is converted into differential through the on-chip balun and followed by a LO driver stage.

The HMC1090LP3E's single-ended RF input is converted into differential through the on-chip balun. The single-ended RF input is internally broadband matched to 50 Ω and requires only a DC-blocking capacitor. Moreover, the HMC1090LP3E's RF input can be externally matched for narrow band applications with a simple matching network, including a series inductor and a shunt capacitor, to further improve the performance. Please refer to the application circuit for narrowband RF input matching for more information.

The HMC1090LP3E's IF amplifier is designed for differential 200 Ω output impedance. As recommended in the application circuit a few external components are required at these IF outputs to acheive a broadband frequency response. Please refer to the IF output interface section for more information. The HMC1090LP3E requires 5V and 3.3V supply voltages and external bias voltages. Bias voltages generate reference currents for the IF and LO amplifiers. The 3.3V supply and the external bias voltages can be generated from the 5V supply in order to operate with a single supply. Please refer to the single supply operation section for more information.

The reference currents to the LO amplifiers and IF amplifiers can be disabled through LOEN and IFEN pins respectively. If the EN pin is connected to LOW or left unconnected, the part operates normally. If the EN pin is connected to HIGH, the LO amplifiers and IF amplifiers are disabled.

Single Supply Operation

The HMC1090LP3E requires 5V and 3.3V supply voltages and external bias voltages. External bias voltages except VGATE pin voltage are already generated from 5V supply voltage on the evaluation board (see application circuit). These bias voltages can be optimized by series resistors with appropriate values from the 5V supply to the bias pins (VCS, LOBIAS1, LOBIAS2). The resistor values on VCS, LOBIAS1 and LOBIAS2 traces on the evaluation board are 240 Ohms, 270 Ohms and 390 Ohms respectively. Refer to the VCS Interface and LOBIAS Interface section for more information.

The nominal VGATE pin voltage is 4.8V, which is applied externally. However, the VGATE pin voltage can be tuned from 4.4V to 5V for optimization of Input IP3 and conversion gain performance. Once optimized, the VGATE pin voltage can be generated from the 5V supply by changing the value of series resistor R13. Please refer to the VGATE interface section for more information.

The 3.3V supply for the LO amplifiers can be generated from the 5V supply by adding a 15 Ohm resistor between LOVDD pin and the 5V supply. Rvdd_lo can be added in series with the LOVDD test point as shown in Figure 1. The resistor must have a power rating of 1/2W or more.

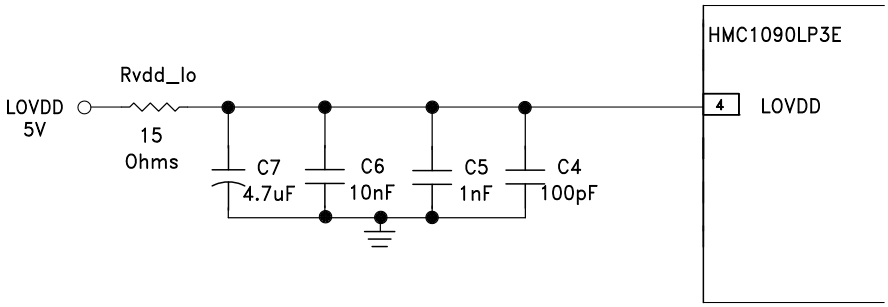


Figure 1. Interface to generate 3.3V for LOVDD pin from the 5V Supply.

VGATE Interface

The VGATE pin is a bias pin for the mixer core. The nominal VGATE pin voltage is 4.8V and is applied externally. This voltage can be tuned from 4.4V to 5V for optimizing input IP3 and conversion gain performance for the desired frequency band. Higher IIP3 values can be obtained by increasing the VGATE pin voltage but this will reduce the conversion gain. Figure-2 shows the measured conversion gain and IIP3 for different values of VGATE.

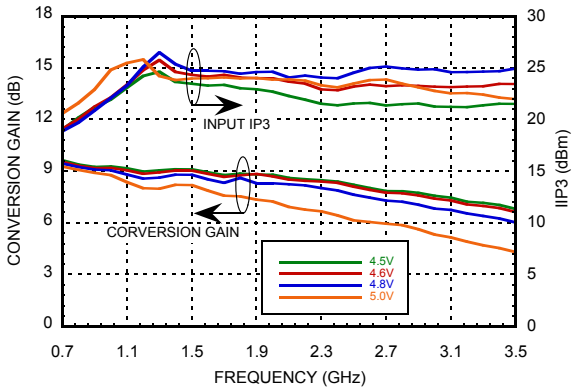


Figure-2. Conversion Gain & IIP3 vs. RF Frequency over VGATE Pin Voltage @25C, IF =150 MHz [1]

[1] Balun losses at IF output ports are de-embedded.

Table-1 shows the typical resistor values to be added in series with VGATE pin to acheive different VGATE voltages.

Table-1:
Resistor values for different VGATE pin voltages

VGATE (V)	R13 (Ohm)
4.4	330
4.5	281
4.6	219
4.7	163
4.8	106
4.9	47
5.0	0

VCS Interface and LOBIAS Interface

The VCS pin is the bias pin for the IF amplifier, which sets the reference current to the IF amplifier. The VCS voltage is generated from the 5V supply by a series resistance. Higher IIP3 values can be obtained by reducing the values of this series resistance R7, which will increase the total supply current of the IF amplifiers. Figure-3a shows the measured conversion gain and IIP3 vs. total supply current from the VBIASIF and VDDIF test points at 1900 MHz.

LOBIAS1 and LOBIAS2 pins are bias pins for LO amplifiers and set the reference currents to these LO amplifiers. The LOBIAS voltage is generated from the 5V supply by series resistances R3 and R1. Figure-3b shows the measured conversion gain and IIP3 vs. total supply current from the VDDLO test point at 1900MHz.

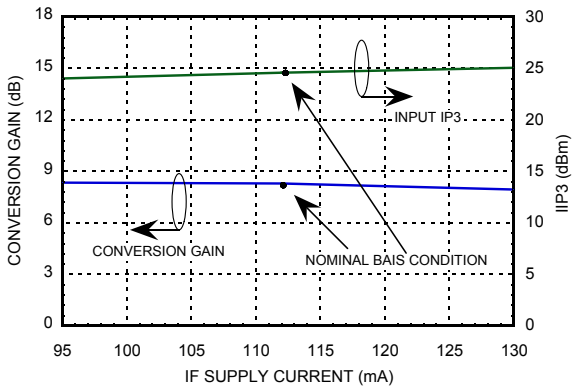


Figure 3a. IIP3 and conversion gain vs. IF stage's Total supply current @ 25° C, RF = 1900 MHz, IF = 150 MHz , VGATE = 4.8V *[1]*

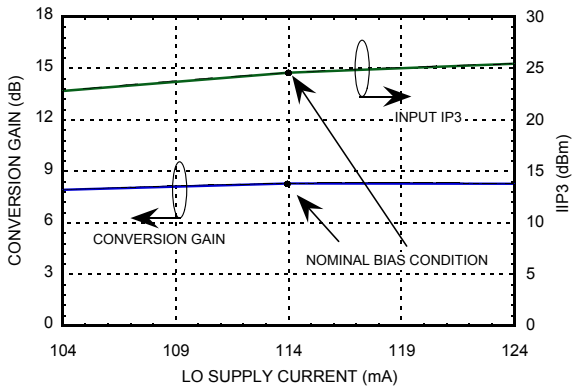


Figure 3b. IIP3 and conversion gain vs. LO stage's Total supply current @ 25° C, RF = 1900 MHz, IF = 150 MHz , VGATE = 4.8V *[1]*

[1] Balun losses at IF output ports are de-embedded.

Table-2 and Table-3 show the typical resistor values that are used in series with VCS, and LOBIAS2 pins for different total supply current values of IF and LO stages. A fine tune for these resistors can be performed if a better fit is required.

Table-2: Resistor Values for Total Supply Current of IF Amplifier

IF Amplifiers Total Supply Current (mA)	R7 (Ohm)
95	510
112	240
130	50

Table-3: Resistor Values for Total Supply Current of LO Amplifier

LO Amplifier Total Supply Current (mA)	R3 (Ohm)
104	1.1K
114	390
124	0

External RF Matching

The HMC1090LP3E's RF input is internally broadband matched to 50Ω. The RF input can be externally matched for a specific RF frequency band of interest to further improve Input IP3 (IIP3). Matching the RF input to a specific RF frequency band can be easily accomplished by adding a series inductor and a shunt capacitor. See Table-4 for values of the external matching components for corresponding RF frequency bands. Figure-4 shows the application circuit with the external components on the RF input pin.

LOBIAS2 and VGATE pin voltages can be optimized for a specific RF frequency band by changing the resistor values in series with these pins. Table-1 shows the resistor value (R13) for corresponding VGATE pin voltages. Table-3 shows the resistor value (R3) for recommended LOBIAS2 pin voltages.

Figure-5 shows the measured conversion gain and IIP3 for 900 MHz,1900 MHz and 2500 MHz RF frequency bands.

Table-4: Components for Selected Frequency Bands

Tune Option	Rmatch	Cmatch1,	Cmatch2	Lmatch	R13	Recommended VGATE Voltages
900 MHz	30 Ohm	Open	Open	0 Ohm	47 Ohm	4.9V
1900 MHz	0 Ohm	1 pF	Open	5.1 nH	163 Ohm	4.7V
2500MHz	0 Ohm	1 pF	Open	3.3 nH	106 Ohm	4.8V

BROADBAND HIGH IP3 DOWNCONVERTER 0.7 - 3.5 GHz

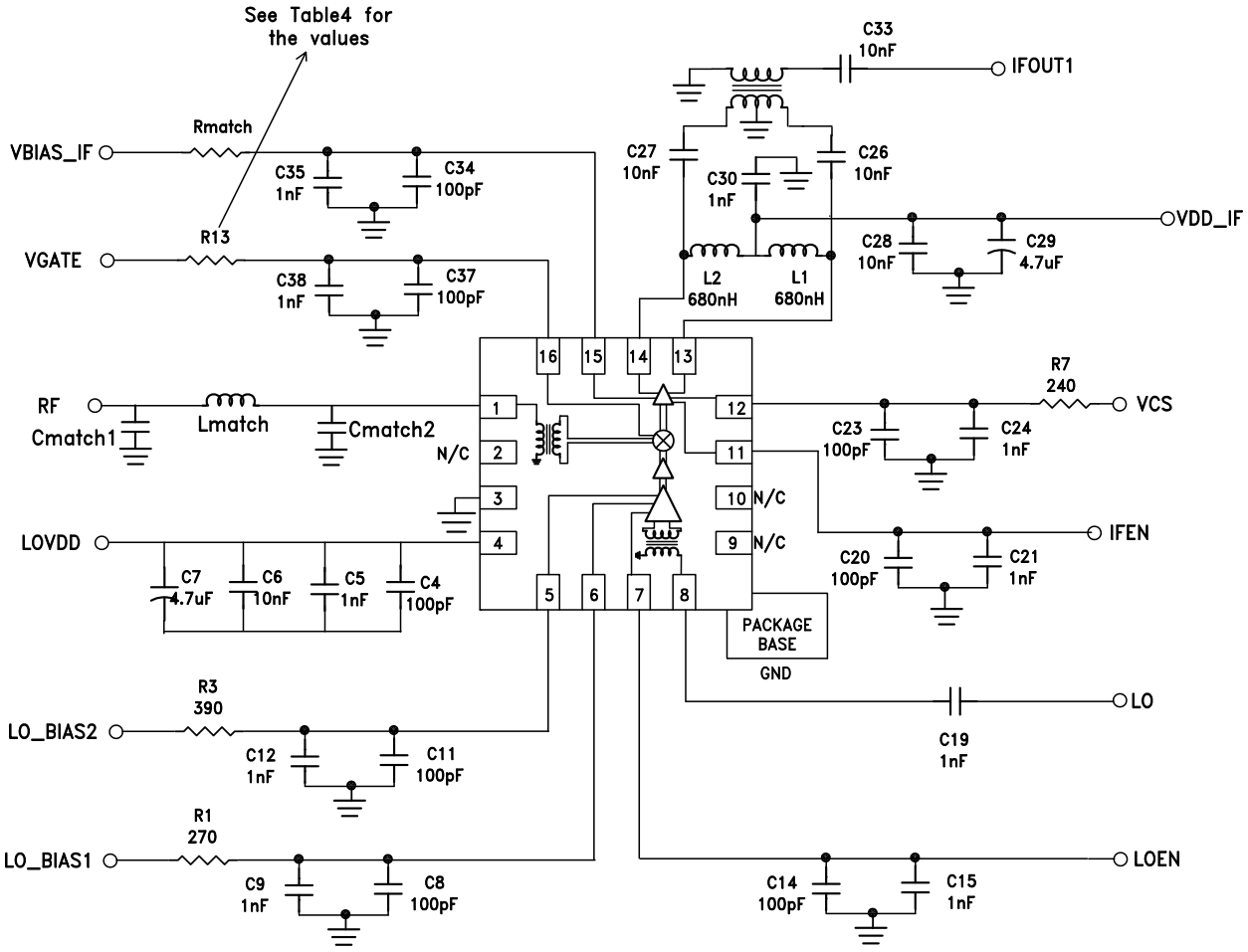


Figure-4. Application Circuit for Narrowband RF Input Matching

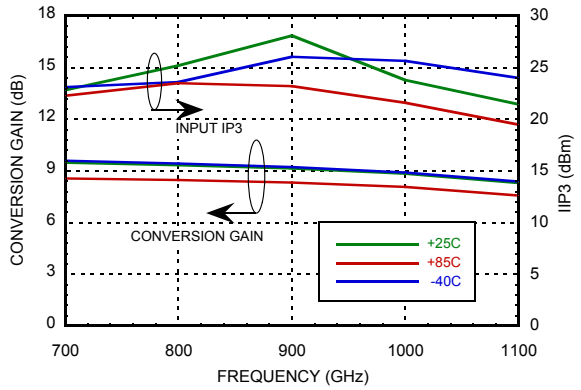


Figure-5a. IIP3 and Conversion Gain with matching for 900 MHz band. Low side LO injection, VGATE = 5.0 V, IF = 100 MHz [1]

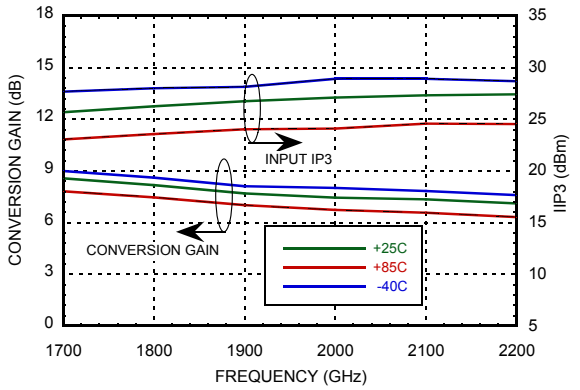


Figure-5b. IIP3 and Conversion Gain with matching for 1900 MHz band, VGATE= 4.7 V, IF= 100 MHz [1]

[1] Balun losses at IF output ports are de-embedded.

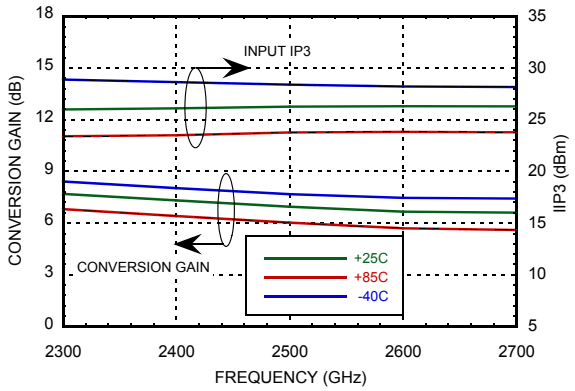


Figure-5c. IIP3 and Conversion Gain with matching for 2500 MHz band VGATE = 4.8 V, IF = 100 MHz [1]

It is recommended to use high side LO injection for RF frequencies below 1 GHz for better IIP3. For instance, higher IIP3 can be obtained if LO input is driven with high side at RF=900 MHz. Please refer to Figure-6.

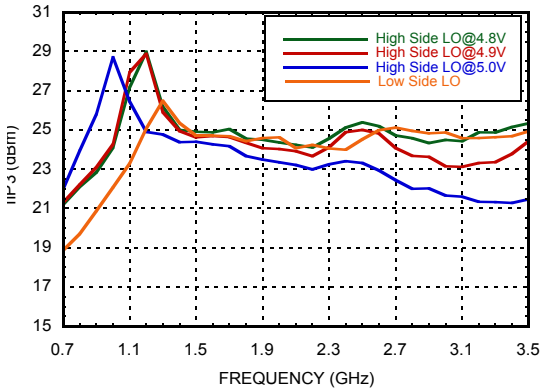


Figure-6. Input IP3 vs. High Side LO & Low Side LO @ VGATE =4.8V

Input IP3 Dependence on RF Input Power

The HMC1090LP3E accepts a wide range of RF input power. Figure-7 shows the IIP3 vs. RF input power for 1900 MHz RF and 150 MHz IF.

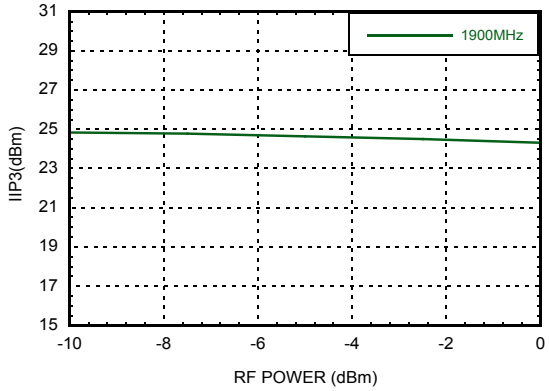


Figure-7. IIP3 vs. RF Input Power, RF = 1900 MHz, IF = 150 MHz, VGATE = 4.8V

[1] Balun losses at IF output ports are de-embedded.

IF Output Interface

The HMC1090LP3E's differential IF output pins are biased at 5V through choke inductors as shown in the application circuit. The default value of these choke inductors is 820 nH. Figure-8 shows the measured conversion gain vs. IF frequency where the 1dB IF bandwidth is approximately 450 MHz and the 3 dB IF bandwidth is above 700 MHz. Higher IF bandwidth values can be obtained by reducing the value of the choke inductors.

Baluns at the IF outputs are used to convert the 200 Ohms differential output impedance of HMC1090LP3E to 50 Ohms single-ended for characterization.

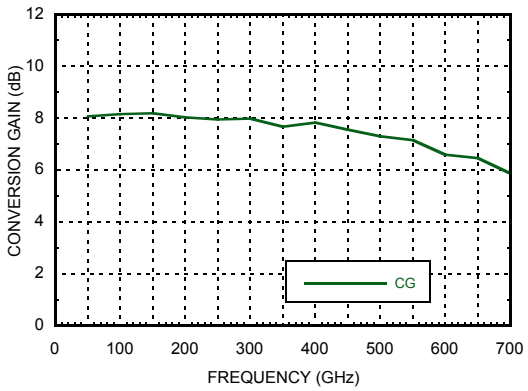


Figure-8. Conversion gain vs. IF Frequency @ LO=1.5 GHz [1]

[1] Balun losses at IF output ports are de-embedded.