



BCM[®] Bus Converter

BCM6123x60E15A3yzz



Fixed Ratio DC-DC Converter

Features

- Up to 130A continuous secondary current
- Up to 2867 W/in³ power density
- 97.4% peak efficiency
- 2,250V_{DC} isolation
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 6123 through-hole ChiP package
 - 2.402" x 0.990" x 0.286"
(61.00mm x 25.14mm x 7.26mm)
- PMBus[™] management interface*

Typical Applications

- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Power Supplies
- Communications Systems
- Transportation

Product Ratings

Product Ratings	
$V_{PRI} = 54V (36 - 60V)$	$I_{SEC} = \text{up to } 130A$
$V_{SEC} = 13.5V (9 - 15V)$ (NO LOAD)	$K = 1/4$

Product Description

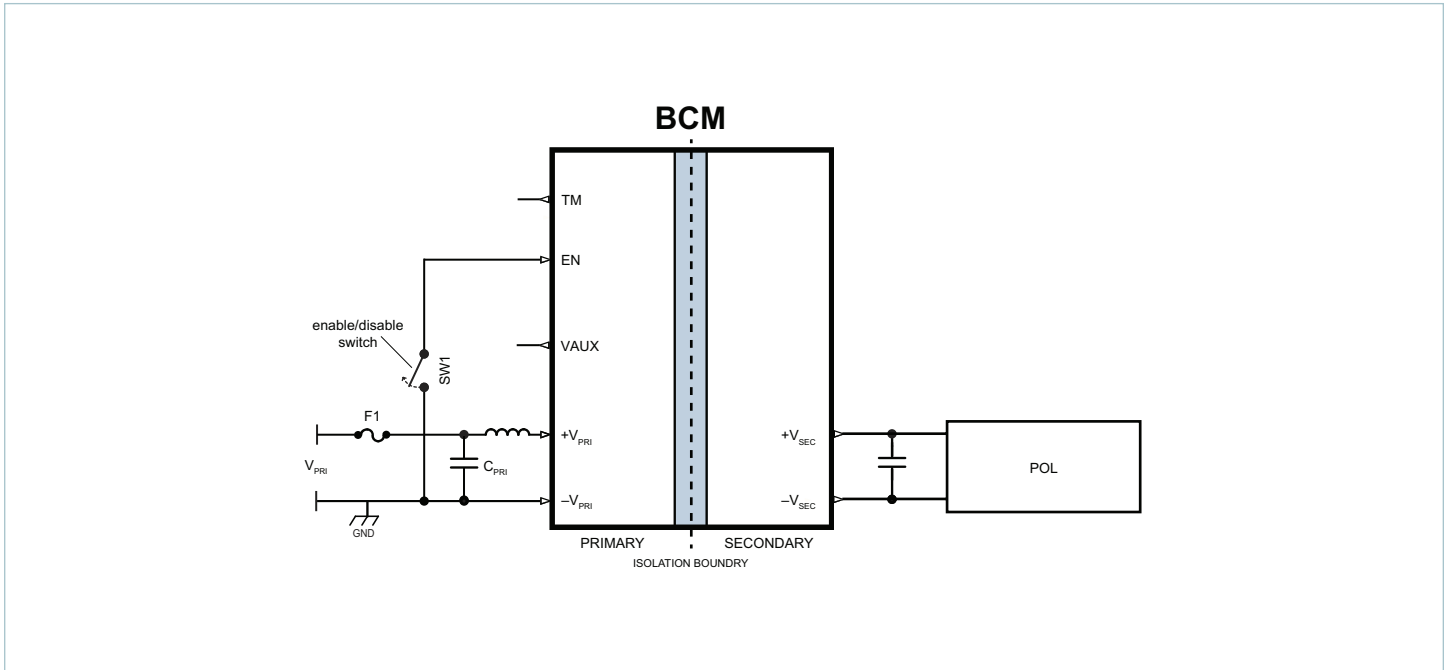
The VI Chip[®] Bus Converter (BCM) is a high efficiency Sine Amplitude Converter[™] (SAC[™]), operating from a 36 to 60V_{DC} primary bus to deliver an isolated, ratiometric secondary voltage from 9 to 15V_{DC}.

The BCM6123x60E15A3yzz offers low noise, fast transient response, and industry leading efficiency and power density. In addition, it provides an AC impedance beyond the bandwidth of most downstream regulators, allowing input capacitance normally located at the input of a POL regulator to be located at the primary side of the BCM module. With a primary to secondary K factor of 1/4, that capacitance value can be reduced by a factor of 16x, resulting in savings of board area, material and total system cost.

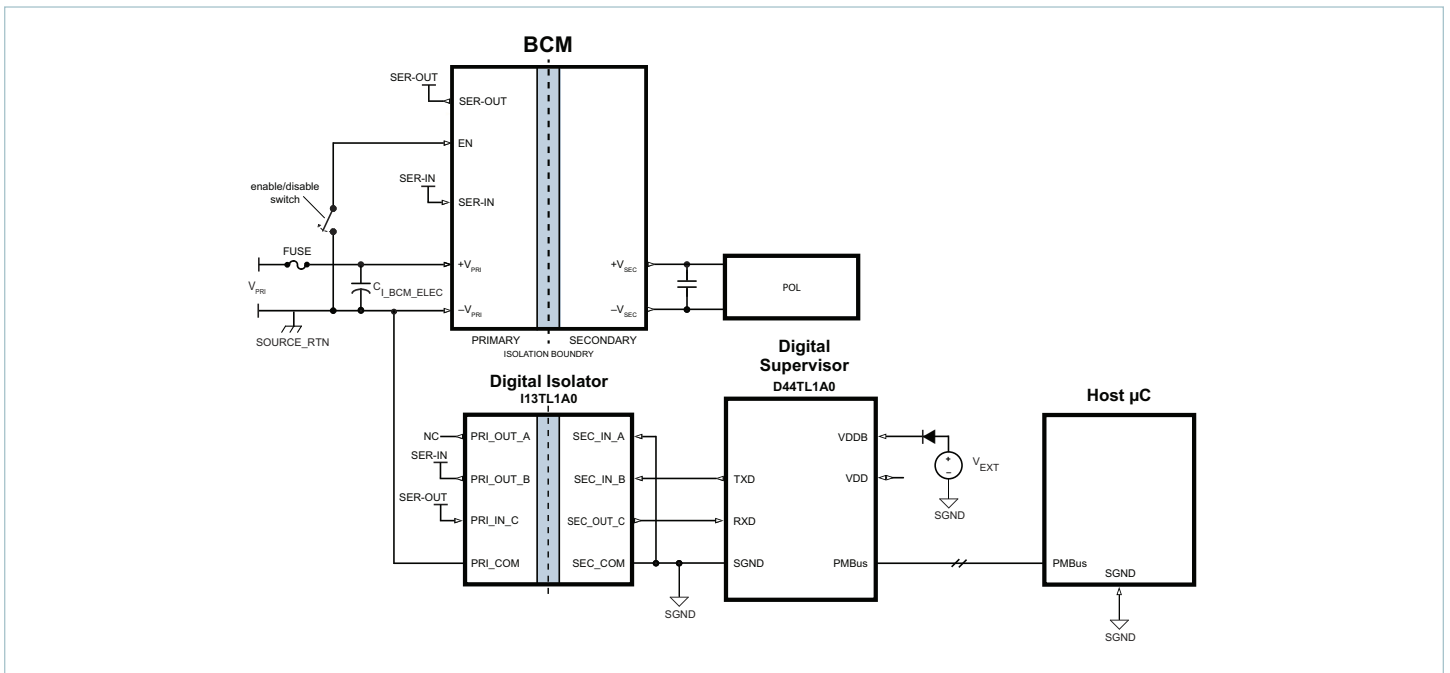
Leveraging the thermal and density benefits of Vicor's ChiP packaging technology, the BCM module offers flexible thermal management options with very low top and bottom side thermal impedances. Thermally-adept ChiP-based power components, enable customers to achieve low cost power system solutions with previously unattainable system size, weight and efficiency attributes, quickly and predictably.

*When used with D44TL1A0 and I13TL1A0 chipset

Typical Application

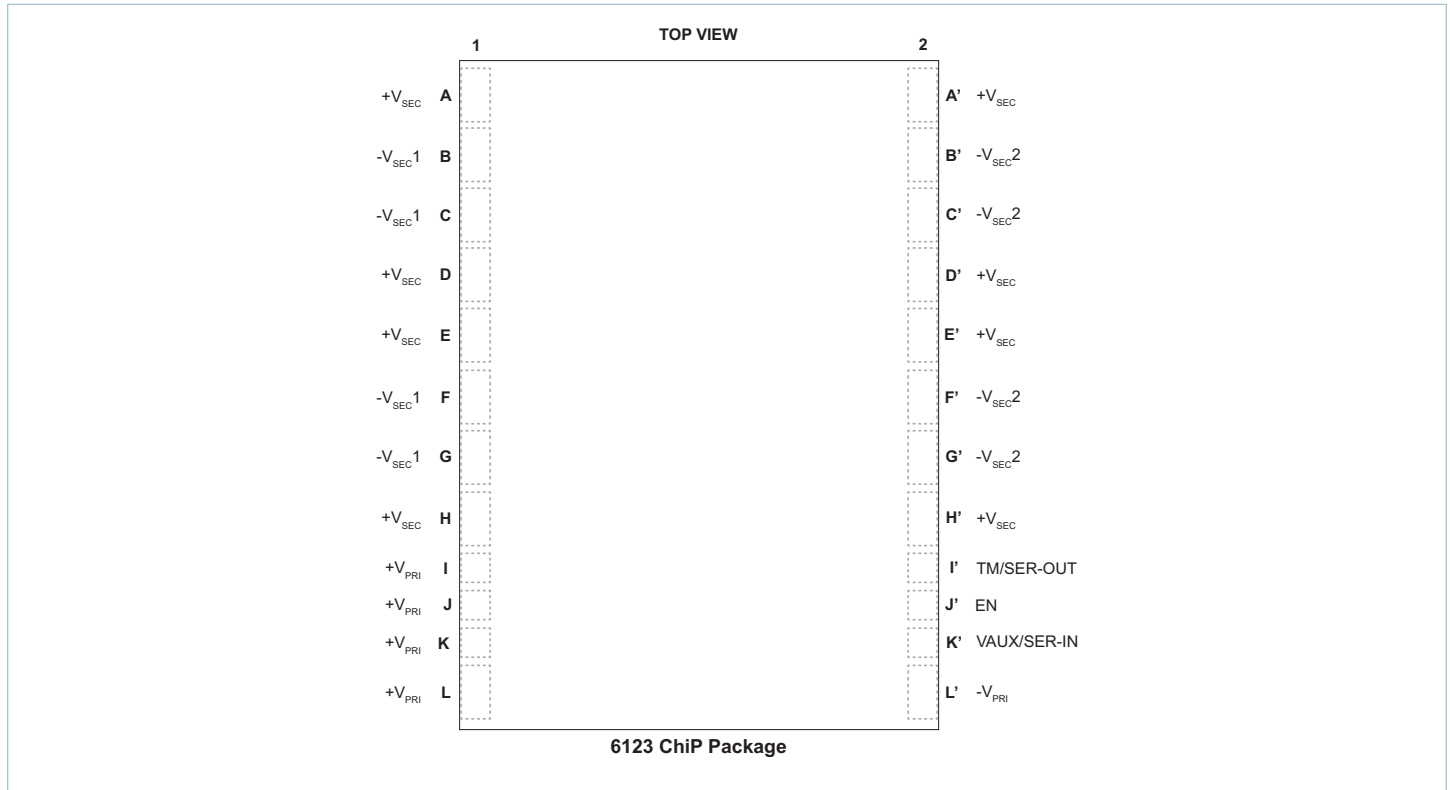


BCM6123x60E15A3y00 at Point of load



BCM6123x60E15A3y01 at Point of load

Pin Configuration



Pin Descriptions

Power Pins			
Pin Number	Signal Name	Type	Function
I1, J1, K1, L1	+V _{PRI}	PRIMARY POWER	Positive primary transformer power terminal
L'2	-V _{PRI}	PRIMARY POWER RETURN	Negative primary transformer power terminal
A1, D1, E1, H1, A'2, D'2, E'2, H'2	+V _{SEC}	SECONDARY POWER	Positive secondary transformer power terminal
B1, C1, F1, G1 B'2, C'2, F'2, G'2	-V _{SEC} *	SECONDARY POWER RETURN	Negative secondary transformer power terminal
Analog Control Signal Pins			
Pin Number	Signal Name	Type	Function
I'2	TM	OUTPUT	Temperature Monitor; primary side referenced signals
J'2	EN	INPUT	Enables and disables power supply; primary side referenced signals
K'2	VAUX	OUTPUT	Auxiliary Voltage Source; primary side referenced signals
PMBus Control Signal Pins			
Pin Number	Signal Name	Type	Function
I'2	SER-OUT	OUTPUT	UART transmit pin; Primary side referenced signals
J'2	EN	INPUT	Enables and disables power supply; Primary side referenced signals
K'2	SER-IN	INPUT	UART receive pin; Primary side referenced signals

*For proper operation an external low impedance connection must be made between listed -V_{SEC1} and -V_{SEC2} terminals.

Part Ordering Information

Product Function	Package Size	Package Mounting	Max Primary Input Voltage	Range Identifier	Max Secondary Voltage	Secondary Output Current	Temperature Grade	Option
BCM	6123	x	60	E	15	A3	y	zz
Bus Converter Module	61 = L 23 = W	T = TH S = SMT	60V	36 – 60V	15V No Load	130A	T = -40°C – 125°C M = -55°C – 125°C	00 = Analog Ctrl 01 = PMBus Ctrl 0R = Reversible Analog Ctrl 0P = Reversible PMBus Ctrl

All products shipped in JEDEC standard high profile (0.400" thick) trays (JEDEC Publication 95, Design Guide 4.10).

Standard Models

Product Function	Package Size	Package Mounting	Max Primary Input Voltage	Range Identifier	Max Secondary Voltage	Secondary Output Current	Temperature Grade	Option
BCM	6123	T	60	E	15	A3	T	00
BCM	6123	T	60	E	15	A3	T	01

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+V _{PRI_DC} to -V _{PRI_DC}		-1	80	V
V _{PRI_DC} or V _{SEC_DC} slew rate (operational)			1	V/μs
+V _{SEC_DC} to -V _{SEC_DC}		-1	20	V
TM / SER-OUT to -V _{PRI_DC}		-0.3	4.6	V
EN to -V _{PRI_DC}			5.5	V
VAUX / SER-IN to -V _{PRI_DC}			4.6	V

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{INTERNAL}} \leq 125^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powetrain PRIMARY to SECONDARY Specification (Forward Direction)						
Primary Input Voltage range, continuous	$V_{\text{PRI_DC}}$		36		60	V
V_{PRI} μ Controller	$V_{\mu\text{C_ACTIVE}}$	$V_{\text{PRI_DC}}$ voltage where μC is initialized, (ie VAUX = Low, powertrain inactive)			14	V
PRI to SEC Input Quiescent Current	$I_{\text{PRI_Q}}$	Disabled, EN Low, $V_{\text{PRI_DC}} = 54\text{V}$ $T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$		5	10	mA
PRI to SEC No Load Power Dissipation	$P_{\text{PRI_NL}}$	$V_{\text{PRI_DC}} = 54\text{V}$, $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$		14.7	21.6	W
		$V_{\text{PRI_DC}} = 54\text{V}$	7		35.2	
		$V_{\text{PRI_DC}} = 36\text{V}$ to 60V , $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$			25	
		$V_{\text{PRI_DC}} = 36\text{V}$ to 60V			38	
PRI to SEC Inrush Current Peak	$I_{\text{PRI_INR_PK}}$	$V_{\text{PRI_DC}} = 60\text{V}$, $C_{\text{SEC_EXT}} = 3000\mu\text{F}$, $R_{\text{LOAD_SEC}} = 20\%$ of full load current		40		A
		$T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$			45	A
DC Primary Input Current	$I_{\text{PRI_IN_DC}}$	At $I_{\text{SEC_OUT_DC}} = 130\text{A}$, $T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$			33	A
Transformation Ratio	K	Primary to secondary, $K = V_{\text{SEC_DC}} / V_{\text{PRI_DC}}$, at no load		1/4		V/V
Secondary Output Current (continuous)	$I_{\text{SEC_OUT_DC}}$				130	A
Secondary Output Current (pulsed)	$I_{\text{SEC_OUT_PULSE}}$	10ms pulse, 25% Duty cycle, $I_{\text{SEC_OUT_AVG}} \leq 50\%$ rated $I_{\text{SEC_OUT_DC}}$			145	A
PRI to SEC Efficiency (ambient)	η_{AMB}	$V_{\text{PRI_DC}} = 54\text{V}$, $I_{\text{SEC_OUT_DC}} = 130\text{A}$	96.2	97		%
		$V_{\text{PRI_DC}} = 36\text{V}$ to 60V , $I_{\text{SEC_OUT_DC}} = 130\text{A}$	95.2			
		$V_{\text{PRI_DC}} = 54\text{V}$, $I_{\text{SEC_OUT_DC}} = 65\text{A}$	96.5	97.4		
PRI to SEC Efficiency (hot)	η_{HOT}	$V_{\text{PRI_DC}} = 54\text{V}$, $I_{\text{SEC_OUT_DC}} = 130\text{A}$	95.8	96.5		%
PRI to SEC Efficiency (over load range)	$\eta_{20\%}$	$26\text{A} < I_{\text{SEC_OUT_DC}} < 130\text{A}$	90			%
PRI to SEC Output Resistance	$R_{\text{SEC_COLD}}$	$V_{\text{PRI_DC}} = 54\text{V}$, $I_{\text{SEC_OUT_DC}} = 130\text{A}$, $T_{\text{INTERNAL}} = -40^{\circ}\text{C}$	1.2	1.5	1.8	m Ω
	$R_{\text{SEC_AMB}}$	$V_{\text{PRI_DC}} = 54\text{V}$, $I_{\text{SEC_OUT_DC}} = 130\text{A}$	1.6	1.95	2.3	
	$R_{\text{SEC_HOT}}$	$V_{\text{PRI_DC}} = 54\text{V}$, $I_{\text{SEC_OUT_DC}} = 130\text{A}$, $T_{\text{INTERNAL}} = 100^{\circ}\text{C}$	2.2	2.5	2.8	
Switching Frequency	F_{SW}	Frequency of the Output Voltage Ripple = $2 \times F_{\text{SW}}$	0.9	0.95	1.0	MHz
Secondary Output Voltage Ripple	$V_{\text{SEC_OUT_PP}}$	$C_{\text{SEC_EXT}} = 0\mu\text{F}$, $I_{\text{SEC_OUT_DC}} = 130\text{A}$, $V_{\text{PRI_DC}} = 54\text{V}$, 20MHz BW		120		mV
		$T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$			250	
Primary Input Leads Inductance (Parasitic)	$L_{\text{PRI_IN_LEADS}}$	Frequency 2.5MHz (double switching frequency), Simulated lead model		6.7		nH
Secondary Output Leads Inductance (Parasitic)	$L_{\text{SEC_OUT_LEADS}}$	Frequency 2.5MHz (double switching frequency), Simulated lead model		0.64		nH

Electrical Specifications (Cont.)

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Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powetrain PRIMARY to SECONDARY Specification (Forward Direction) Cont.						
Effective Primary Capacitance (Internal)	$C_{\text{PRI_INT}}$	Effective Value at $54V_{\text{PRI_DC}}$		11.2		μF
Effective Secondary Capacitance (Internal)	$C_{\text{SEC_INT}}$	Effective Value at $13.5V_{\text{SEC_DC}}$		140		μF
Effective Secondary Output Capacitance (External)	$C_{\text{SEC_OUT_EXT}}$	Excessive capacitance may drive module into SC protection			3000	μF
Effective Secondary Output Capacitance (External)	$C_{\text{SEC_OUT_AEXT}}$	$C_{\text{SEC_OUT_AEXT MAX}} = N * 0.5 * C_{\text{SEC_OUT_EXT MAX}}$, where N = the number of units in parallel				
Powertrain Protection PRIMARY to SECONDARY (Forward Direction)						
Auto Restart Time	$t_{\text{AUTO_RESTART}}$	Startup into a persistent fault condition. Non-Latching fault detection given $V_{\text{PRI_DC}} > V_{\text{PRI_UVLO+}}$	490		560	ms
Primary Overvoltage Lockout Threshold	$V_{\text{PRI_OVLO+}}$		63	67	71	V
Primary Overvoltage Recovery Threshold	$V_{\text{PRI_OVLO-}}$		61	65	69	V
Primary Overvoltage Lockout Hysteresis	$V_{\text{PRI_OVLO_HYST}}$			2		V
Primary Overvoltage Lockout Response Time	$t_{\text{PRI_OVLO}}$			100		μs
Primary Soft-Start Time	$t_{\text{PRI_SOFT-START}}$	From powertrain active. Fast Current limit protection disabled during Soft-Start		1		ms
Secondary Output Overcurrent Trip Threshold	$I_{\text{SEC_OUT_OCP}}$		145	180	225	A
Secondary Output Overcurrent Response Time Constant	$t_{\text{SEC_OUT_OCP}}$	Effective internal RC filter		3		ms
Secondary Output Short Circuit Protection Trip Threshold	$I_{\text{SEC_OUT_SCP}}$		195			A
Secondary Output Short Circuit Protection Response Time	$t_{\text{SEC_OUT_SCP}}$			1		μs
Overtemperature Shutdown Threshold	$t_{\text{OTP+}}$	Temperature sensor located inside controller IC	125			$^{\circ}\text{C}$

Electrical Specifications (Cont.)

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Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Supervisory Limits PRIMARY to SECONDARY (Forward Direction)						
Primary Overvoltage Lockout Threshold	$V_{\text{PRI_OVLO+}}$		64	66	68	V
Primary Overvoltage Recovery Threshold	$V_{\text{PRI_OVLO-}}$		60	64	66	V
Primary Overvoltage Lockout Hysteresis	$V_{\text{PRI_OVLO_HYST}}$			2		V
Primary Overvoltage Lockout Response Time	$t_{\text{PRI_OVLO}}$			100		μs
Primary Undervoltage Lockout Threshold	$V_{\text{PRI_UVLO-}}$		26	28	30	V
Primary Undervoltage Recovery Threshold	$V_{\text{PRI_UVLO+}}$		28	30	32	V
Primary Undervoltage Lockout Hysteresis	$V_{\text{PRI_UVLO_HYST}}$			2		V
Primary Undervoltage Lockout Response Time	$t_{\text{PRI_UVLO}}$			100		μs
Primary Undervoltage Startup Delay	$t_{\text{PRI_UVLO+_DELAY}}$	From $V_{\text{PRI_DC}} = V_{\text{PRI_UVLO+}}$ to powertrain active, EN floating, (i.e One time Startup delay form application of $V_{\text{PRI_DC}}$ to $V_{\text{SEC_DC}}$)		20		ms
Secondary Output Overcurrent Trip Threshold	$I_{\text{SEC_OUT_OCP}}$		164	176	188	A
Secondary Output Overcurrent Response Time Constant	$t_{\text{SEC_OUT_OCP}}$	Effective internal RC filter		3		ms
Overtemperature Shutdown Threshold	$t_{\text{OTP+}}$	Temperature sensor located inside controller IC	125			$^{\circ}\text{C}$
Overtemperature Recovery Threshold	$t_{\text{OTP-}}$		105	110	115	$^{\circ}\text{C}$
Undertemperature Shutdown Threshold	t_{UTP}	Temperature sensor located inside controller IC; Protection not available for M-Grade units.			-45	$^{\circ}\text{C}$
Undertemperature Restart Time	$t_{\text{UTP_RESTART}}$	Startup into a persistent fault condition. Non-Latching fault detection given $V_{\text{PRI_DC}} > V_{\text{PRI_UVLO+}}$		3		s

Electrical Specifications (Cont.)

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Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powetrain SECONDARY to PRIMARY Specification (Reverse Direction)						
Secondary Input Voltage range, continuous	$V_{\text{SEC_DC}}$		9		15	V
SEC to PRI No Load Power Dissipation	$P_{\text{SEC_NL}}$	$V_{\text{SEC_DC}} = 13.5\text{V}, T_{\text{INTERNAL}} = 25^{\circ}\text{C}$		14.7	21.6	W
		$V_{\text{SEC_DC}} = 13.5\text{V}$	7		35.2	
		$V_{\text{SEC_DC}} = 9\text{V to } 15\text{V}, T_{\text{INTERNAL}} = 25^{\circ}\text{C}$			25	
		$V_{\text{SEC_DC}} = 9\text{V to } 15\text{V}$			38	
DC Secondary Input Current	$I_{\text{SEC_IN_DC}}$	At $I_{\text{PRI_DC}} = 32.5\text{A}, T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$			132.5	A
Primary Output Current (continuous)	$I_{\text{PRI_OUT_DC}}$				32.5	A
Primary Output Current (pulsed)	$I_{\text{PRI_OUT_PULSE}}$	10ms pulse, 25% Duty cycle, $I_{\text{PRI_OUT_AVG}} \leq 50\%$ rated $I_{\text{PRI_OUT_DC}}$			39	A
SEC to PRI Efficiency (ambient)	η_{AMB}	$V_{\text{SEC_DC}} = 13.5\text{V}, I_{\text{PRI_OUT_DC}} = 32.5\text{A}$	96.2	97.0		%
		$V_{\text{SEC_DC}} = 9\text{V to } 15\text{V}, I_{\text{PRI_OUT_DC}} = 32.5\text{A}$	95.2			
		$V_{\text{SEC_DC}} = 13.5\text{V}, I_{\text{PRI_OUT_DC}} = 16.25\text{A}$	96.5	97.4		
SEC to PRI Efficiency (hot)	η_{HOT}	$V_{\text{SEC_DC}} = 13.5\text{V}, I_{\text{PRI_OUT_DC}} = 32.5\text{A}$	95.8	96.5		%
SEC to PRI Efficiency (over load range)	$\eta_{20\%}$	$6.5\text{A} < I_{\text{PRI_OUT_DC}} < 32.5\text{A}$	92			%
SEC to PRI Output Resistance	$R_{\text{PRI_COLD}}$	$V_{\text{SEC_DC}} = 13.5\text{V}, I_{\text{PRI_OUT_DC}} = 32.5\text{A}, T_{\text{INTERNAL}} = -40^{\circ}\text{C}$	25	30	35	m Ω
	$R_{\text{PRI_AMB}}$	$V_{\text{SEC_DC}} = 13.5\text{V}, I_{\text{PRI_OUT_DC}} = 32.5\text{A}$	31	38	45	
	$R_{\text{PRI_HOT}}$	$V_{\text{SEC_DC}} = 13.5\text{V}, I_{\text{PRI_OUT_DC}} = 32.5\text{A}, T_{\text{INTERNAL}} = 100^{\circ}\text{C}$	41	47	53	
Primary Output Voltage Ripple	$V_{\text{PRI_OUT_PP}}$	$C_{\text{PRI_OUT_EXT}} = 0\mu\text{F}, I_{\text{PRI_OUT_DC}} = 32.5\text{A}, V_{\text{SEC_DC}} = 13.5\text{V}, 20\text{MHz BW}$		500		mV
		$T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$			1000	

Electrical Specifications (Cont.)

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Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Protection SECONDARY to PRIMARY (Reverse Direction)						
Effective Primary Output Capacitance (External)	$C_{\text{PRI_OUT_EXT}}$	Excessive capacitance may drive module into SC protection			100	μF
Secondary Overvoltage Lockout Threshold	$V_{\text{SEC_OVLO+}}$	Module latched shutdown with $V_{\text{PRI_DC}} < V_{\text{PRI_UVLO-R}}$	16	16.5	17.3	V
Secondary Overvoltage Lockout Response Time	$t_{\text{PRI_OVLO}}$			100		μs
Secondary Undervoltage Lockout Threshold	$V_{\text{SEC_UVLO-}}$	Module latched shutdown with $V_{\text{PRI_DC}} < V_{\text{PRI_UVLO-R}}$	6.5	7	7.5	V
Secondary Undervoltage Lockout Response Time	$t_{\text{SEC_UVLO}}$			100		μs
Primary Undervoltage Lockout Threshold	$V_{\text{PRI_UVLO-R}}$	Applies only to reversilbe products in forward and in reverse direction; $I_{\text{PRI_DC}} \leq 20$ while $V_{\text{PRI_UVLO-R}} < V_{\text{PRI_DC}} < V_{\text{PRI_MIN}}$	26	28	30	V
Primary Undervoltage Recovery Threshold	$V_{\text{PRI_UVLO+R}}$	Applies only to reversilbe products in forward and in reverse direction;	28	30	32	V
Primary Undervoltage Lockout Hysteresis	$V_{\text{PRI_UVLO_HYST_R}}$	Applies only to reversilbe products in forward and in reverse direction;		2		V
Primary Output Overcurrent Trip Threshold (Analog)	$I_{\text{PRI_OUT_OCP}}$	Module latched shutdown with $V_{\text{PRI_DC}} < V_{\text{PRI_UVLO-R}}$	36.25	45	56.25	A
Primary Output Overcurrent Response Time Constant (Analog)	$t_{\text{PRI_OUT_OCP}}$	Effective internal RC filter		3		ms
Primary Short Circuit Protection Trip Threshold	$I_{\text{PRI_SCP}}$	Module latched shutdown with $V_{\text{PRI_DC}} < V_{\text{PRI_UVLO-R}}$	48.75			A
Primary Short Circuit Protection Response Time	$t_{\text{PRI_SCP}}$			1		μs
Primary Output Overcurrent Trip Threshold (PM Bus)	$I_{\text{PRI_OUT_OCP}}$	Module latched shutdown with $V_{\text{PRI_DC}} < V_{\text{PRI_UVLO-R}}$	41	44	47	A
Primary Output Overcurrent Response Time Constant (PM Bus)	$t_{\text{PRI_OUT_OCP}}$	Effective internal RC filter		3		ms

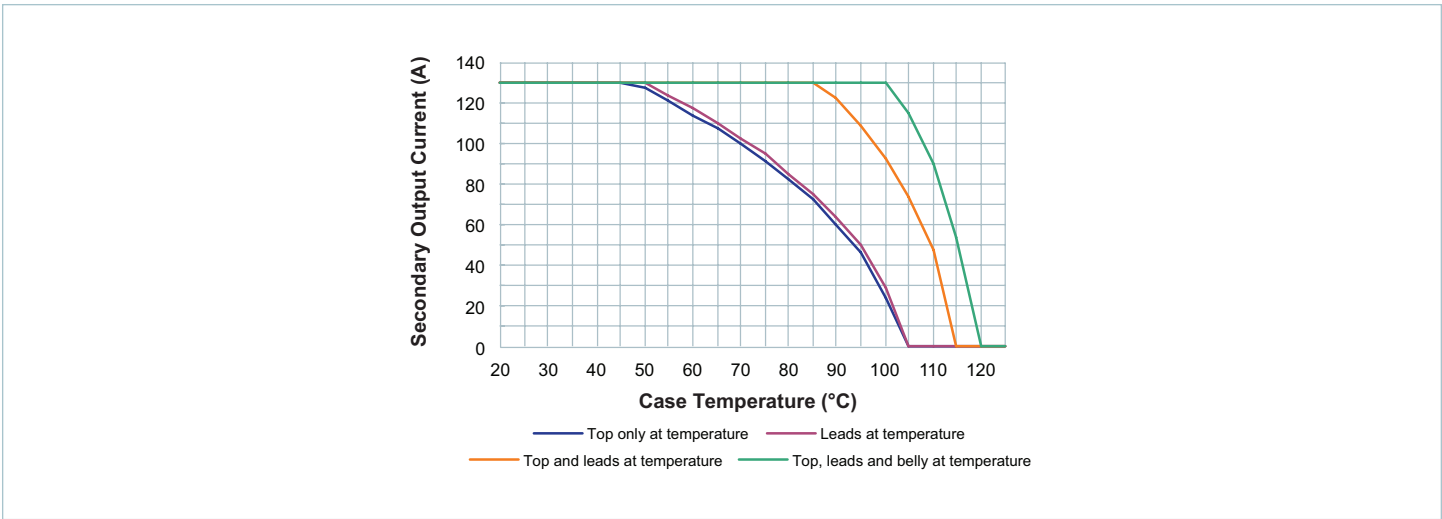


Figure 1 — Specified thermal operating area

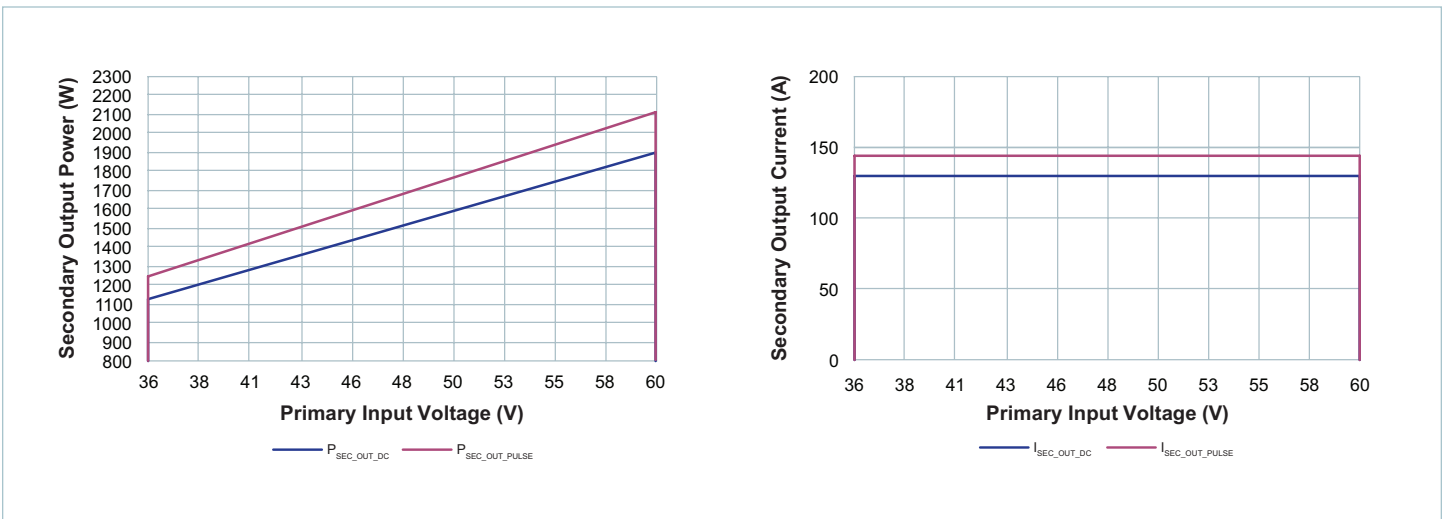


Figure 2 — Specified electrical operating area using rated R_{SEC_HOT}

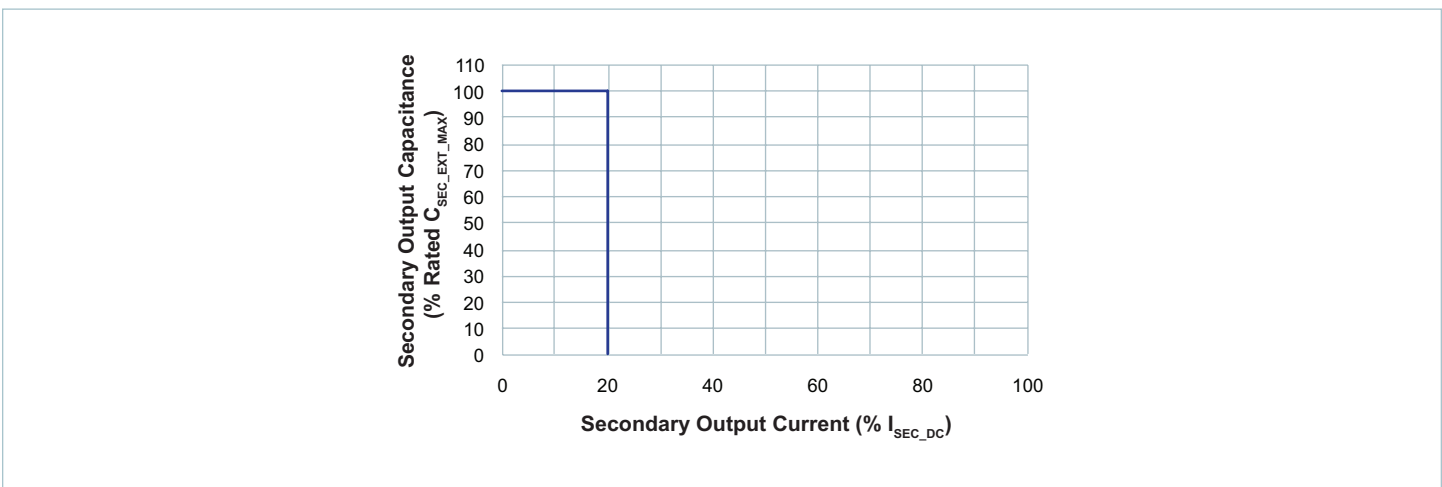


Figure 3 — Specified Primary start-up into load current and external capacitance

Analog Control Signal Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{INTERNAL}} \leq 125^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ unless otherwise noted.

Temperature Monitor									
<ul style="list-style-type: none"> The TM pin is a standard analog I/O configured as an output from an internal μC. The TM pin monitors the internal temperature of the controller IC within an accuracy of $\pm 5^{\circ}\text{C}$. μC 250kHz PWM output internally pulled high to 3.3V. 									
SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT	
DIGITAL OUTPUT	Startup	Powertrain active to TM time	t_{TM}			100		μs	
		TM Duty Cycle	TM_{PWM}		18.18		68.18	%	
	Regular Operation	TM Current	I_{TM}					4	mA
		Recommended External filtering							
		TM Capacitance (External)	$C_{\text{TM_EXT}}$	Recommended External filtering			0.01		μF
		TM Resistance (External)	$R_{\text{TM_EXT}}$	Recommended External filtering			1		$\text{k}\Omega$
		Specifications using recommended filter							
		TM Gain	A_{TM}				10		$\text{mV} / ^{\circ}\text{C}$
		TM Voltage Reference	$V_{\text{TM_AMB}}$				1.27		V
		TM Voltage Ripple	$V_{\text{TM_PP}}$	$R_{\text{TM_EXT}} = 1\text{K Ohm}, C_{\text{TM_EXT}} = 0.01\mu\text{F}, V_{\text{PRI_DC}} = 54\text{V}, I_{\text{SEC_DC}} = 130\text{A}$			28		mV
		$T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$				40			

Enable / Disable Control								
<ul style="list-style-type: none"> The EN pin is a standard analog I/O configured as an input to an internal μC. It is internally pulled high to 3.3V. When held low the BCM internal bias will be disabled and the powertrain will be inactive. In an array of BCMS, EN pins should be interconnected to synchronize startup. 								
SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	Startup	EN to Powertrain active time	$t_{\text{EN_START}}$	$V_{\text{PRI_DC}} > V_{\text{PRI_UVLO+}}$, EN held low both conditions satisfied for $T > t_{\text{PRI_UVLO+_DELAY}}$		250		μs
		EN Voltage Threshold	$V_{\text{EN_TH}}$		2.3			V
	Regular Operation	EN Resistance (Internal)	$R_{\text{EN_INT}}$	Internal pull up resistor		1.5		$\text{k}\Omega$
		EN Disable Threshold	$V_{\text{EN_DISABLE_TH}}$					1

Analog Control Signal Characteristics (Cont.)

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{INTERNAL}} \leq 125^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ unless otherwise noted.

Auxiliary Voltage Source									
<ul style="list-style-type: none"> The VAUX pin is a standard analog I/O configured as an output from an internal μC. VAUX is internally connected to μC output as internally pulled high to a 3.3V regulator with 2% tolerance, a 1% resistor of 1.5kΩ. VAUX can be used as a "Ready to process full power" flag. This pin transitions VAUX voltage after a 2ms delay from the start of powertrain activating, signaling the end of softstart. VAUX can be used as "Fault flag". This pin is pulled low internally when a fault protection is detected. 									
SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT	
ANALOG OUTPUT	Startup	Powertrain active to VAUX time	t_{VAUX}	Powertrain active to VAUX High		2		ms	
	Regular Operation	VAUX Voltage	V_{VAUX}		2.8		3.3	V	
		VAUX Available Current	I_{VAUX}				4	mA	
		VAUX Voltage Ripple	$V_{\text{VAUX_PP}}$	$T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$		50		100	mV
		VAUX Capacitance (External)	$C_{\text{VAUX_EXT}}$					0.01	μF
	VAUX Resistance (External)	$R_{\text{VAUX_EXT}}$	$V_{\text{PRI_DC}} < V_{\mu\text{C_ACTIVE}}$		1.5			k Ω	
Fault	VAUX Fault Response Time	$t_{\text{VAUX_FR}}$		From fault to $V_{\text{VAUX}} = 2.8\text{V}$, $C_{\text{VAUX}} = 0\text{pF}$		10		μs	

PMBus™ Control Signal Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{INTERNAL}} \leq 125^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ unless otherwise noted.

UART SER-IN / SER-OUT Pins									
<ul style="list-style-type: none"> • Universal Asynchronous Receiver/Transmitter (UART) pins. • The BCM communication version is not intended to be used without a Digital Supervisor. • Isolated I²C communication and telemetry is available when using Vicor Digital Isolator and Vicor Digital Supervisor. Please see specific product data sheet for more details. • UART SER-IN pin is internally pulled high using a 1.5kΩ to 3.3V. 									
SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT	
GENERAL I/O	Regular Operation	Baud Rate	BR _{UART}	Rate		750		Kbit/s	
DIGITAL INPUT		SER-IN Pin							
		SER-IN Input Voltage Range	V _{SER-IN_IH}			2.3			V
			V _{SER-IN_IL}					1	V
		SER-IN rise time	t _{SER-IN_RISE}		10% to 90%		400		ns
		SER-IN fall time	t _{SER-IN_FALL}		10% to 90%		25		ns
		SER-IN R _{PULLUP}	R _{SER-IN_PLP}		Pull up to 3.3V		1.5		kΩ
SER-IN External Capacitance		C _{SER-IN_EXT}					400	pF	
DIGITAL OUTPUT		SER-OUT Pin							
		SER-OUT Output Voltage Range	V _{SER-OUT_OH}		0mA ≥ I _{OH} ≥ -4mA	2.8			V
			V _{SER-OUT_OL}		0mA ≤ I _{OL} ≤ 4mA			0.5	V
		SER-OUT rise time	t _{SER-OUT_RISE}		10% to 90%		55		ns
		SER-OUT fall time	t _{SER-OUT_FALL}		10% to 90%		45		ns
		SER-OUT source current	I _{SER-OUT}		V _{SER-OUT} = 2.8V			6	mA
SER-OUT output impedance	Z _{SER-OUT}					120	Ω		

Enable / Disable Control									
<ul style="list-style-type: none"> • The EN pin is a standard analog I/O configured as an input to an internal μC. • It is internally pulled high to 3.3V. • When held low the BCM internal bias will be disabled and the powertrain will be inactive. • In an array of BCMs, EN pins should be interconnected to synchronize startup. • Enable / disable command will have no effect if the EN pin is disabled. 									
SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT	
ANALOG INPUT	Startup	EN to Powertrain active time	t _{EN_START}	V _{PRL_DC} > V _{PRL_UVLO+} , EN held low both conditions satisfied for t > t _{PRL_UVLO+_DELAY}		250		μs	
	Regular Operation	EN Voltage Threshold	V _{ENABLE}		2.3			V	
		EN Resistance (Internal)	R _{EN_INT}	Internal pull up resistor			1.5		kΩ
		EN Disable Threshold	V _{EN_DISABLE_TH}					1	V

PMBus™ Reported Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{INTERNAL}} \leq 125^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ unless otherwise noted.

Monitored Telemetry					
• The BCM communication version is not intended to be used without a Digital Supervisor.					
ATTRIBUTE	DIGITAL SUPERVISOR PMBus™ READ COMMAND	ACCURACY (RATED RANGE)	FUNCTIONAL REPORTING RANGE	UPDATE RATE	REPORTED UNITS
Input voltage	(88h) READ_VIN	± 5% (LL - HL)	28V to 66V	100µs	$V_{\text{ACTUAL}} = V_{\text{REPORTED}} \times 10^{-1}$
Input current	(89h) READ_IIN	± 20% (10 - 20% of FL) ± 5% (20 - 133% of FL)	-44A to 44A	100µs	$I_{\text{ACTUAL}} = I_{\text{REPORTED}} \times 10^{-2}$
Output voltage ^[1]	(8Bh) READ_VOUT	± 5%(LL - HL)	7.0V to 16.5V	100µs	$V_{\text{ACTUAL}} = V_{\text{REPORTED}} \times 10^{-1}$
Output current	(8Ch) READ_IOUT	± 20% (10 - 20% of FL) ± 5% (20 - 133% of FL)	-176A to 176A	100µs	$I_{\text{ACTUAL}} = I_{\text{REPORTED}} \times 10^{-2}$
Output resistance	(D4h) READ_ROUT	± 5% (50 - 100% of FL) at NL ± 10% (50 - 100% of FL)(LL - HL)	1000u to 3000u	100ms	$R_{\text{ACTUAL}} = R_{\text{REPORTED}} \times 10^{-5}$
Temperature ^[2]	(8Dh) READ_TEMPERATURE_1	± 7°C(Full Range)	- 55°C to 130°C	100ms	$T_{\text{ACTUAL}} = T_{\text{REPORTED}}$

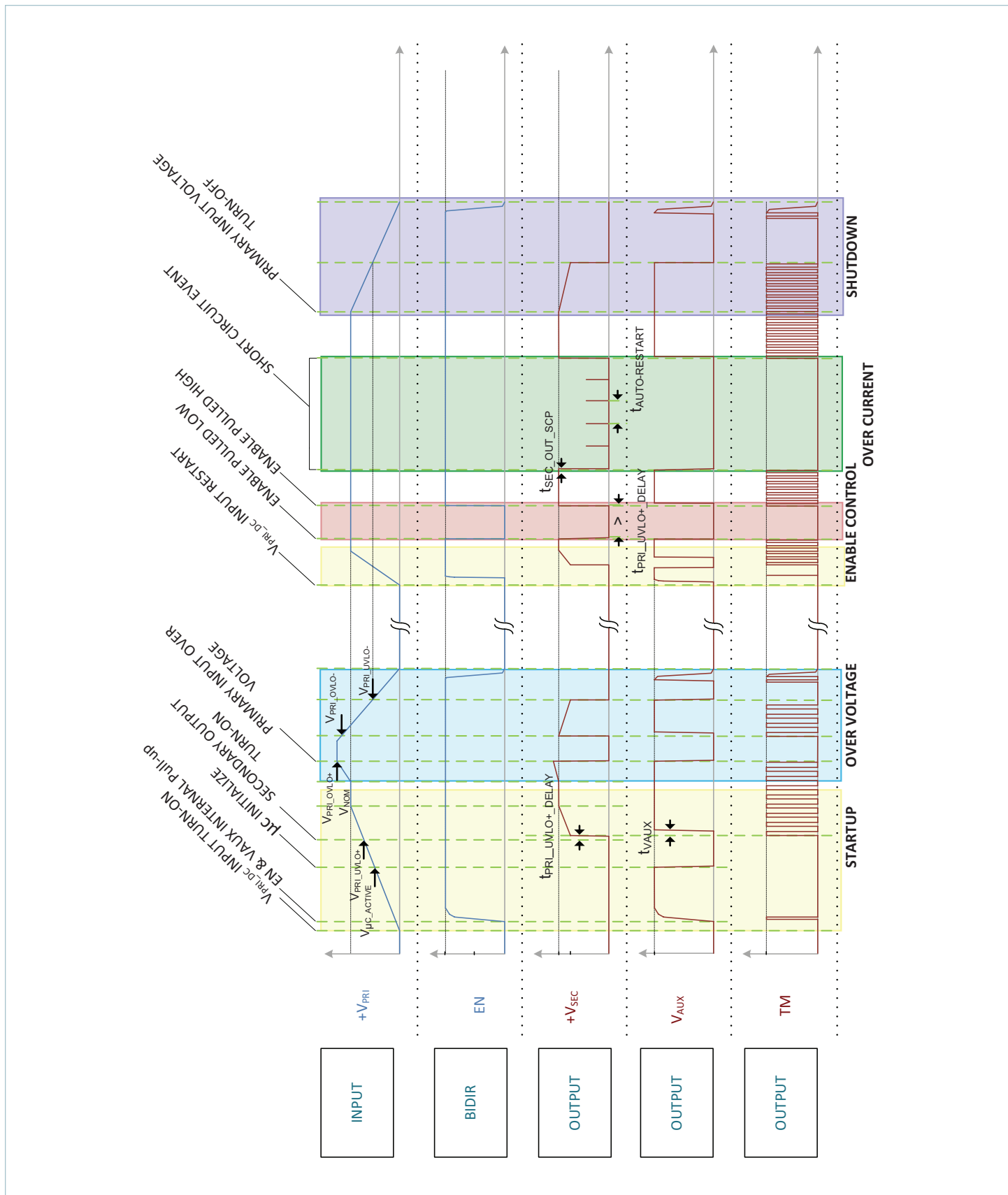
^[1] Default READ Output Voltage returned when unit is disabled = -300 V.

^[2] Default READ Temperature returned when unit is disabled = -273°C.

Variable Parameter					
<ul style="list-style-type: none"> • Factory setting of all below Thresholds and Warning limits are 100% of listed protection values. • Variables can be written only when module is disabled either EN pulled low or $V_{\text{IN}} < V_{\text{IN_UVLO}}$. • Module must remain in a disabled mode for 3 ms after any changes to the below variables allowing ample time to commit changes to EEPROM. 					
ATTRIBUTE	DIGITAL SUPERVISOR PMBus™ COMMAND ^[3]	CONDITIONS / NOTES	ACCURACY (RATED RANGE)	FUNCTIONAL REPORTING RANGE	DEFAULT VALUE
Input / Output Overvoltage Protection Limit	(55h) VIN_OV_FAULT_LIMIT	$V_{\text{IN_OVLO}}$ is automatically 3% lower than this set point	± 5% (LL - HL)	28V to 66V	100%
Input / Output Overvoltage Warning Limit	(57h) VIN_OV_WARN_LIMIT		± 5% (LL - HL)	28V to 66V	100%
Input / Output Undervoltage Protection Limit	(D7h) DISABLE_FAULTS	Can only be disabled to a preset default value	± 5% (LL - HL)	28V or 66V	100%
Input Overcurrent Protection Limit	(58h) IIN_OC_FAULT_LIMIT		± 20% (10 - 20% of FL) ± 5% (20 - 133% of FL)	0 to 44A	100%
Input Overcurrent Warning Limit	(5Dh) IIN_OC_WARN_LIMIT		± 20% (10 - 20% of FL) ± 5% (20 - 133% of FL)	0 to 44A	100%
Overtemperature Protection Limit	(4Fh) OT_FAULT_LIMIT		± 7°C (Full Range)	0 to 125°C	100%
Overtemperature Warning Limit	(51h) OT_WARN_LIMIT		± 7°C (Full Range)	0 to 125°C	100%
Turn on Delay	(60h) TON_DELAY	Additional time delay to the Undervoltage Startup Delay	± 50µs	0 to 100ms	0ms

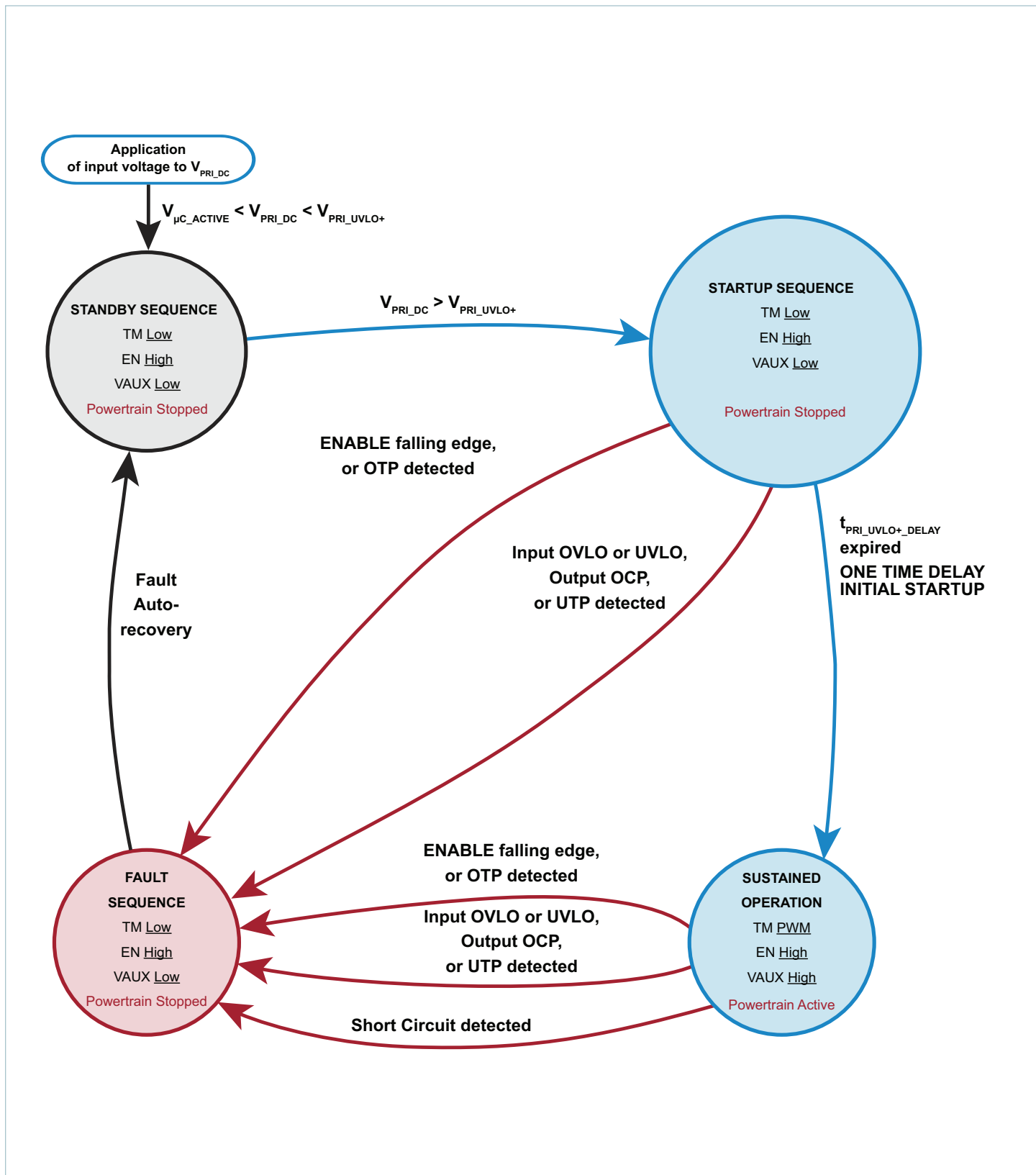
^[3] Refer to Digital Supervisor datasheet for complete list of supported commands.

BCM Module Timing diagram



High Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.



Application Characteristics

Product is mounted and temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected data from primary sourced units processing power in forward direction. See associated figures for general trend data.

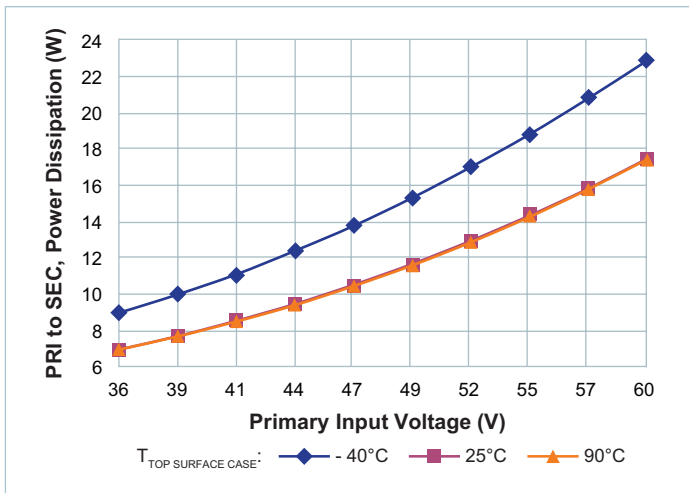


Figure 4 — No load power dissipation vs. V_{PRI_DC}

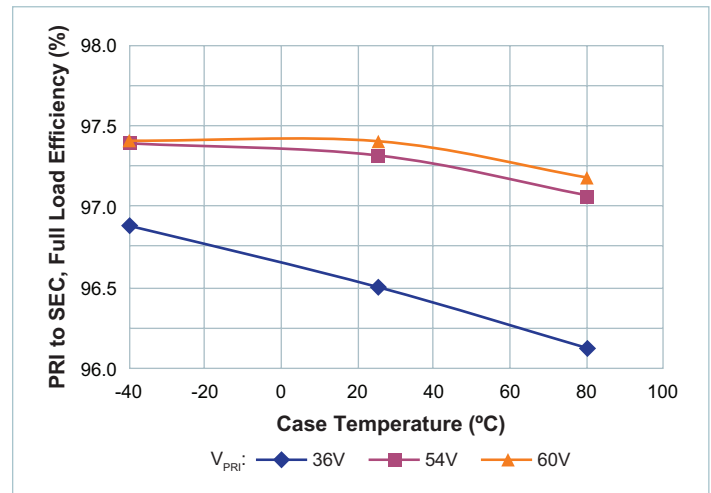


Figure 5 — Full load efficiency vs. temperature; V_{PRI_DC}

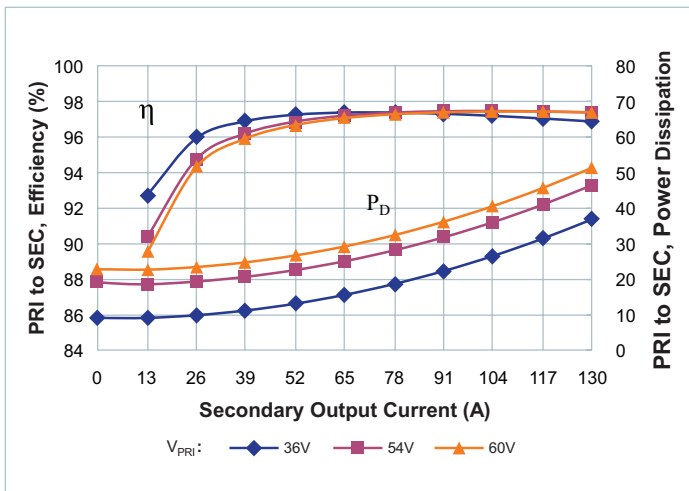


Figure 6 — Efficiency and power dissipation at $T_{CASE} = -40^\circ C$

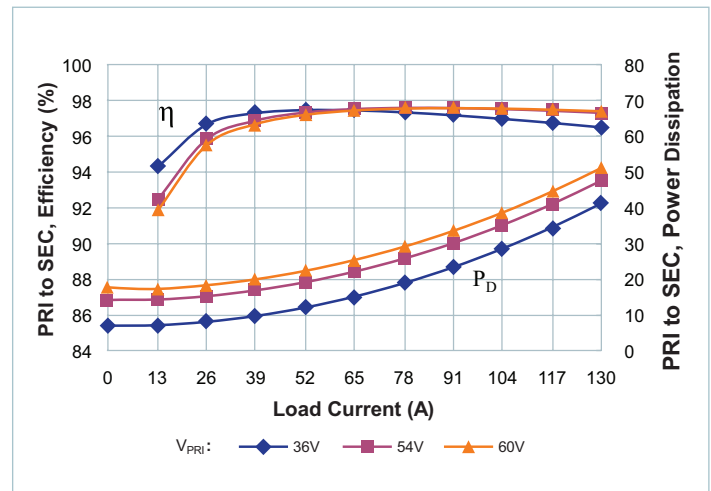


Figure 7 — Efficiency and power dissipation at $T_{CASE} = 25^\circ C$

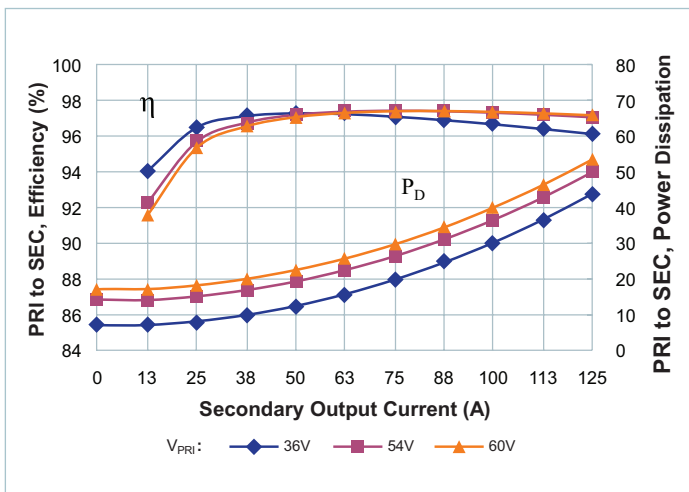


Figure 8 — Efficiency and power dissipation at $T_{CASE} = 80^\circ C$

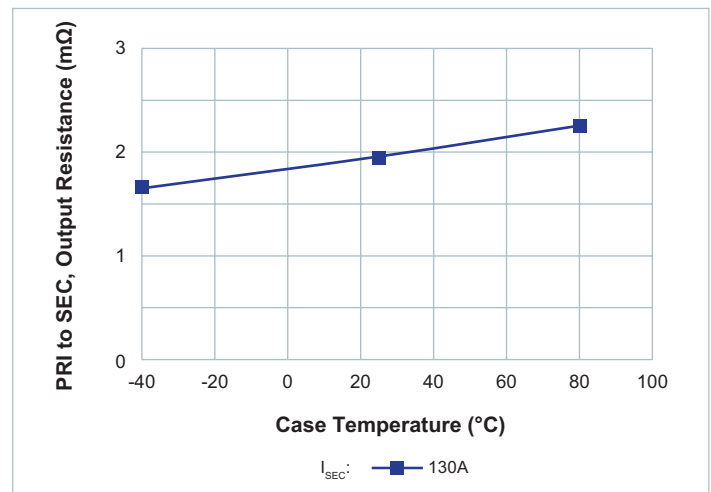


Figure 9 — R_{SEC} vs. temperature; Nominal V_{PRI_DC}
 $I_{SEC_DC} = 125A$ at $T_{CASE} = 80^\circ C$

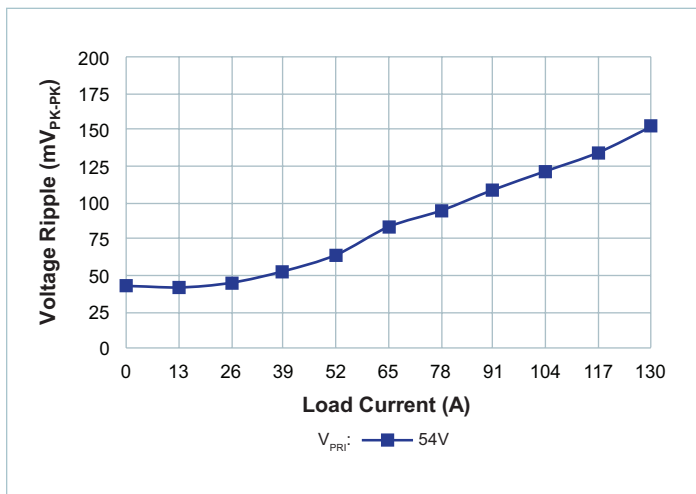


Figure 10 — $V_{SEC_OUT_PP}$ vs. I_{SEC_DC} ; No external $C_{SEC_OUT_EXT}$. Board mounted module, scope setting: 20MHz analog BW

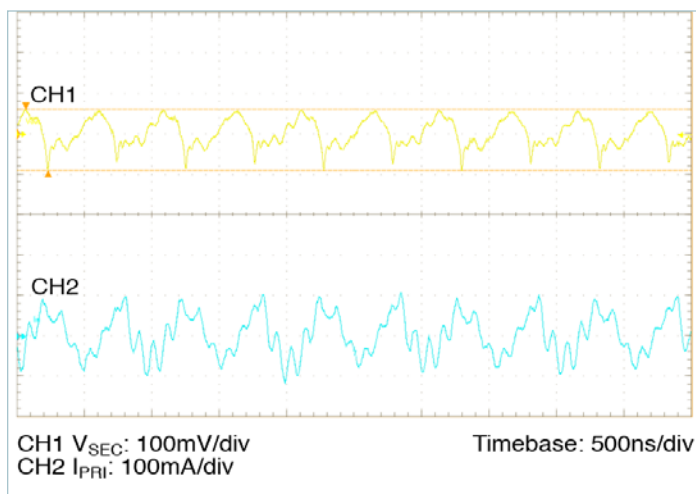


Figure 11 — Full load ripple, 2700 μ F $C_{PRI_IN_EXT}$; No external $C_{SEC_OUT_EXT}$. Board mounted module, scope setting: 20MHz analog BW

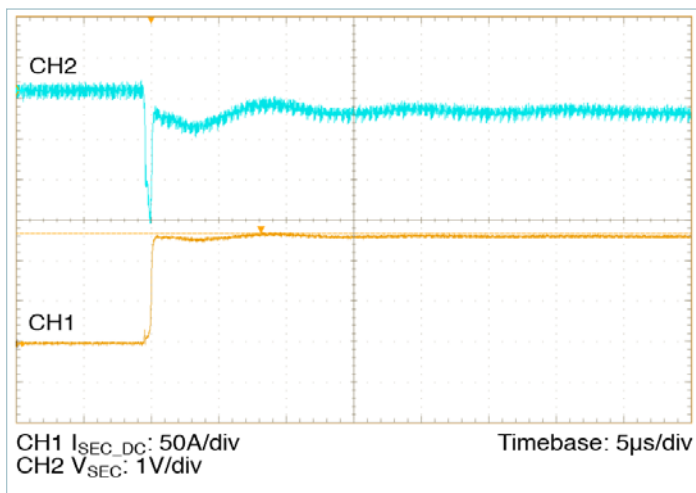


Figure 12 — 0A – 130A transient response: $C_{PRI_IN_EXT} = 2700\mu$ F, no external $C_{SEC_OUT_EXT}$

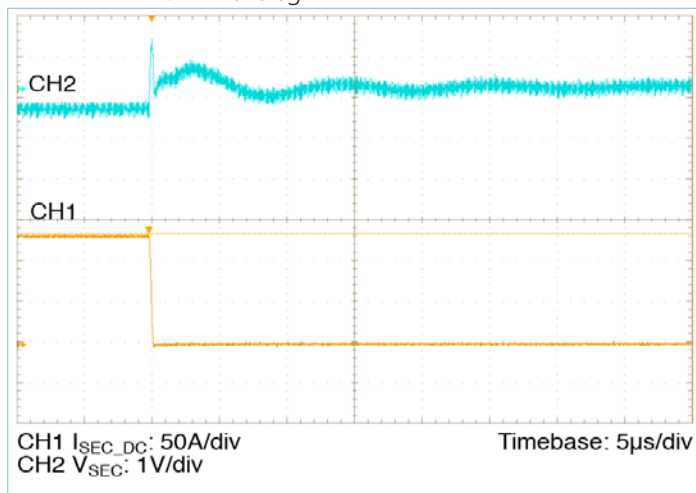


Figure 13 — 130A – 0A transient response: $C_{PRI_IN_EXT} = 2700\mu$ F, no external $C_{SEC_OUT_EXT}$

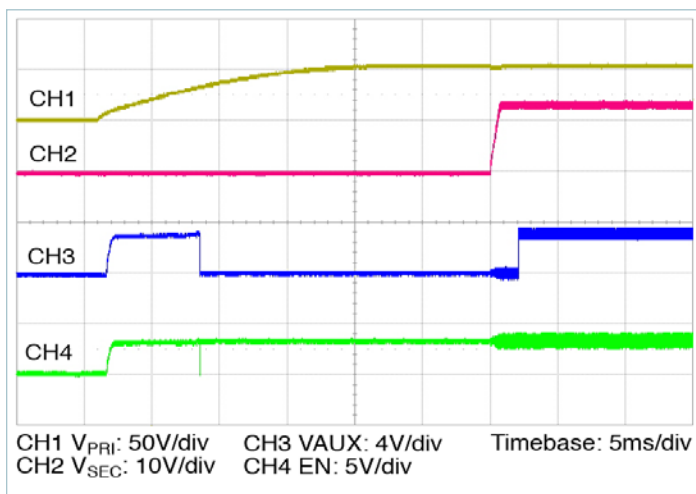


Figure 14 — Start up from application of $V_{PRI_DC} = 54V$, 20% I_{OUT} , 100% $C_{SEC_OUT_EXT}$

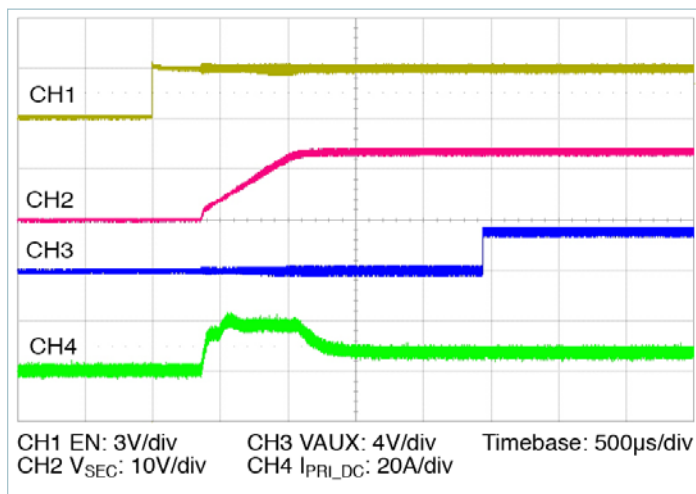


Figure 15 — Start up from application of EN with pre-applied $V_{PRI_DC} = 54V$, 20% I_{SEC_DC} , 100% $C_{SEC_OUT_EXT}$

General Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{INTERNAL}} \leq 125^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		60.87 / [2.396]	61.00 / [2.402]	61.13 / [2.407]	mm/[in]
Width	W		24.76 / [0.975]	25.14 / [0.990]	25.52 / [1.005]	mm/[in]
Height	H		7.21 / [0.284]	7.26 / [0.286]	7.31 / [0.288]	mm/[in]
Volume	Vol	Without Heatsink		11.13 / [0.679]		cm ³ /[in ³]
Weight	W			41 / [1.45]		g/[oz]
Lead finish		Nickel	0.51		2.03	μm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
Thermal						
Operating Temperature	T _{INTERNAL}	BCM6123x60E15A3yzz (T-Grade)	-40		125	°C
Thermal Resistance Top Side	Φ _{INT-TOP}	Estimated thermal resistance to maximum temperature internal component from isothermal top		1.26		°C/W
Thermal Resistance Leads	Φ _{INT-LEADS}	Estimated thermal resistance to maximum temperature internal component from isothermal leads		1.21		°C/W
Thermal Resistance Bottom Side	Φ _{INT-BOTTOM}	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		1.03		°C/W
Thermal Capacity				34		Ws/°C
Assembly						
Storage temperature		BCM6123x60E15A3yzz (T-Grade)	-55		125	°C
ESD Withstand	ESD _{HBM}	Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2kV)				
	ESD _{CDM}	Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V)				

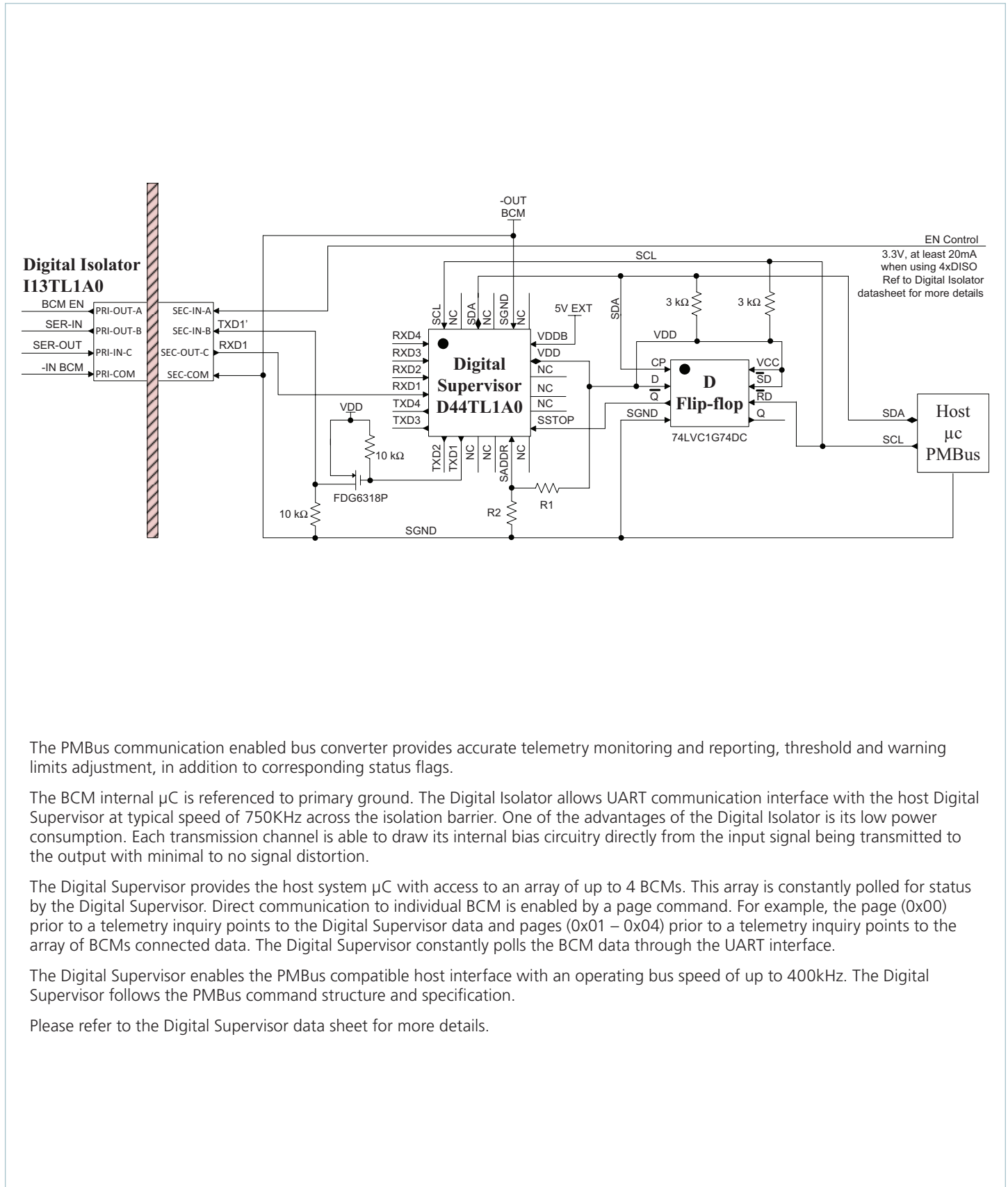
General Characteristics (Cont.)

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{INTERNAL}} \leq 125^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ unless otherwise noted.

Soldering ^[1]						
Peak Temperature Top Case					135	°C
Safety						
Isolation voltage / Dielectric test	V _{HIPO} T	PRIMARY to SECONDARY	2,250			V _{DC}
		PRIMARY to CASE	2,250			
		SECONDARY to CASE	707			
Isolation Capacitance	C _{PRI_SEC}	Unpowered Unit	620	780	940	pF
Insulation Resistance	R _{PRI_SEC}	At 500 Vdc	10			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer		4.45		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		7.01		MHrs
Agency Approvals / Standards		cTÜVus "EN 60950-1"				
		cURus "UL 60950-1"				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

^[1] Product is not intended for reflow solder attach.

PMBus™ System Diagram



The PMBus communication enabled bus converter provides accurate telemetry monitoring and reporting, threshold and warning limits adjustment, in addition to corresponding status flags.

The BCM internal μC is referenced to primary ground. The Digital Isolator allows UART communication interface with the host Digital Supervisor at typical speed of 750KHz across the isolation barrier. One of the advantages of the Digital Isolator is its low power consumption. Each transmission channel is able to draw its internal bias circuitry directly from the input signal being transmitted to the output with minimal to no signal distortion.

The Digital Supervisor provides the host system μC with access to an array of up to 4 BCMs. This array is constantly polled for status by the Digital Supervisor. Direct communication to individual BCM is enabled by a page command. For example, the page (0x00) prior to a telemetry inquiry points to the Digital Supervisor data and pages (0x01 – 0x04) prior to a telemetry inquiry points to the array of BCMs connected data. The Digital Supervisor constantly polls the BCM data through the UART interface.

The Digital Supervisor enables the PMBus compatible host interface with an operating bus speed of up to 400kHz. The Digital Supervisor follows the PMBus command structure and specification.

Please refer to the Digital Supervisor data sheet for more details.

Sine Amplitude Converter™ Point of Load Conversion

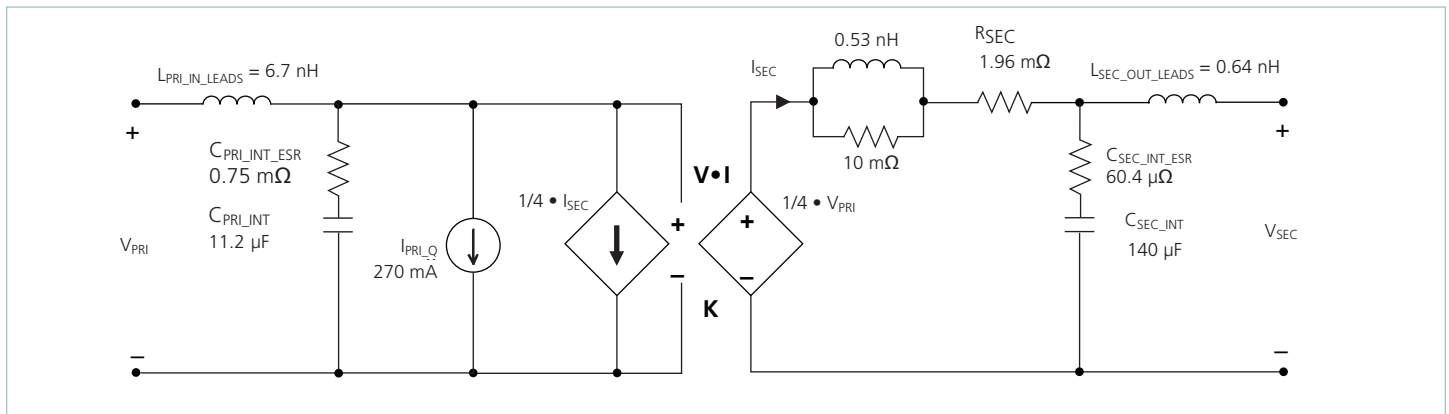


Figure 16 — BCM module AC model

The Sine Amplitude Converter (SAC™) uses a high frequency resonant tank to move energy from Primary to secondary and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of primary voltage and secondary current. A small amount of capacitance embedded in the primary and secondary stages of the module is sufficient for full functionality and is key to achieving high power density.

The BCM6123x60E15A3yzz SAC can be simplified into the preceding model.

At no load:

$$V_{SEC} = V_{PRI} \cdot K \tag{1}$$

K represents the “turns ratio” of the SAC. Rearranging Eq (1):

$$K = \frac{V_{SEC}}{V_{PRI}} \tag{2}$$

In the presence of load, V_{SEC} is represented by:

$$V_{SEC} = V_{PRI} \cdot K - I_{SEC} \cdot R_{SEC} \tag{3}$$

and I_{SEC} is represented by:

$$I_{SEC} = \frac{I_{PRI} - I_{PRI_Q}}{K} \tag{4}$$

R_{SEC} represents the impedance of the SAC, and is a function of the R_{DS(on)} of the primary and secondary MOSFETs and the winding resistance of the power transformer. PRI_Q represents the quiescent current of the SAC control, gate drive circuitry, and core losses.

The use of DC voltage transformation provides additional

interesting attributes. Assuming that R_{SEC} = 0Ω and I_{PRI_Q} = 0A, Eq. (3) now becomes Eq. (1) and is essentially load independent, resistor R is now placed in series with P_{RI}.

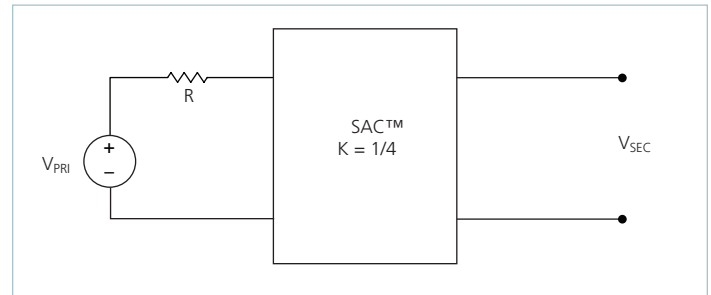


Figure 17 — K = 1/4 Sine Amplitude Converter with series primary resistor

The relationship between V_{PRI} and V_{SEC} becomes:

$$V_{SEC} = (V_{PRI} - I_{PRI} \cdot R) \cdot K \tag{5}$$

Substituting the simplified version of Eq. (4) (I_{PRI_Q} is assumed = 0A) into Eq. (5) yields:

$$V_{SEC} = V_{PRI} \cdot K - I_{SEC} \cdot R \cdot K^2 \tag{6}$$

This is similar in form to Eq. (3), where R_{SEC} is used to represent the characteristic impedance of the SAC™. However, in this case a real R on the primary side of the SAC is effectively scaled by K² with respect to the secondary.

Assuming that R = 1Ω, the effective R as seen from the secondary side is 62.5mΩ, with K = 1/4 .

A similar exercise should be performed with the addition of a capacitor or shunt impedance at the primary of the SAC. A switch in series with V_{PRI} is added to the circuit. This is depicted in Figure 18.

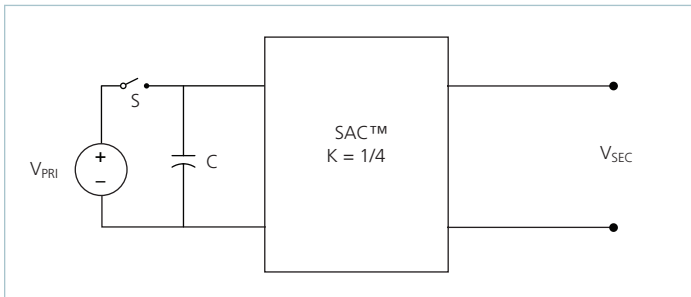


Figure 18 — Sine Amplitude Converter with primary capacitor

A change in V_{PRI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C \frac{dV_{PRI}}{dt} \quad (7)$$

Assume that with the capacitor charged to V_{PRI} , the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{SEC} \cdot K \quad (8)$$

substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{SEC} = \frac{C}{K^2} \cdot \frac{dV_{SEC}}{dt} \quad (9)$$

The equation in terms of the secondary has yielded a K^2 scaling factor for C , specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the secondary when expressed in terms of the primary. With a $K = 1/4$ as shown in Figure 18, $C = 1\mu\text{F}$ would appear as $C = 16\mu\text{F}$ when viewed from the secondary.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e. well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM module are:

- No load power dissipation (P_{PRI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss (R_{SEC}): refers to the power loss across the BCM module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{PRI_NL} + P_{R_{SEC}} \quad (10)$$

Therefore,

$$P_{SEC_OUT} = P_{PRI_IN} - P_{DISSIPATED} = P_{PRI_IN} - P_{PRI_NL} - P_{R_{SEC}} \quad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\begin{aligned} \eta &= \frac{P_{SEC_OUT}}{P_{PRI_IN}} = \frac{P_{PRI_IN} - P_{PRI_NL} - P_{R_{SEC}}}{P_{PRI_IN}} \quad (12) \\ &= \frac{V_{PRI} \cdot I_{PRI} - P_{PRI_NL} - (I_{SEC})^2 \cdot R_{SEC}}{V_{PRI} \cdot I_{PRI}} \\ &= 1 - \left(\frac{P_{PRI_NL} + (I_{SEC})^2 \cdot R_{SEC}}{V_{PRI} \cdot I_{PRI}} \right) \end{aligned}$$

Input and Output Filter Design

A major advantage of SAC™ systems versus conventional PWM converters is that the transformer based SAC does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of primary voltage and secondary current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the primary and secondary stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- Guarantee low source impedance:

To take full advantage of the BCM module’s dynamic response, the impedance presented to its primary terminals must be low from DC to approximately 5MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100nH, the primary should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200nH, the RC damper may be as high as 1µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

- Further reduce primary and/or secondary voltage ripple without sacrificing dynamic response:

Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the primary source will appear at the secondary of the module multiplied by its K factor.

- Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:

The module primary/secondary voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating primary range. Even when disabled, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it.

Total load capacitance at the secondary of the BCM module shall not exceed the specified maximum. Owing to the wide bandwidth and low secondary impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the primary of the module. At frequencies <500kHz the module appears as an impedance of R_{SEC} between the source and load.

Within this frequency range, capacitance at the primary appears as effective capacitance on the secondary per the relationship defined in Eq. (13).

$$C_{SEC_EXT} = \frac{C_{PRI_EXT}}{K^2} \quad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Thermal Considerations

The ChiP package provides a high degree of flexibility in that it presents three pathways to remove heat from internal power dissipating components. Heat may be removed from the top surface, the bottom surface and the leads. The extent to which these three surfaces are cooled is a key component for determining the maximum power that is available from a ChiP, as can be seen from Figure 1.

Since the ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a real thermal solution. Given that there are three pathways to remove heat from the ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 19 shows the “thermal circuit” for a VI Chip® BCM module 6123 in an application where the top, bottom, and leads are cooled. In this case, the BCM power dissipation is PD_{TOTAL} and the three surface temperatures are represented as T_{CASE_TOP}, T_{CASE_BOTTOM}, and T_{LEADS}. This thermal system can now be very easily analyzed using a SPICE simulator with simple resistors, voltage sources, and a current source. The results of the simulation would provide an estimate of heat flow through the various pathways as well as internal temperature.

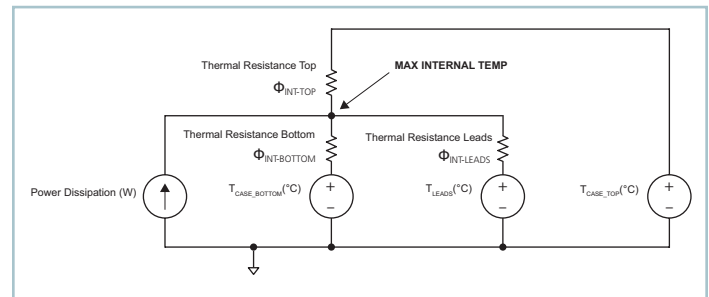


Figure 19 — Top case, Bottom case and leads thermal model

Alternatively, equations can be written around this circuit and analyzed algebraically:

$$\begin{aligned} T_{INT} - PD_1 \cdot \Phi_{INT-TOP} &= T_{CASE_TOP} \\ T_{INT} - PD_2 \cdot \Phi_{INT-BOTTOM} &= T_{CASE_BOTTOM} \\ T_{INT} - PD_3 \cdot \Phi_{INT-LEADS} &= T_{LEADS} \\ PD_{TOTAL} &= PD_1 + PD_2 + PD_3 \end{aligned}$$

Where T_{INT} represents the internal temperature and PD₁, PD₂, and PD₃ represent the heat flow through the top side, bottom side, and leads respectively.

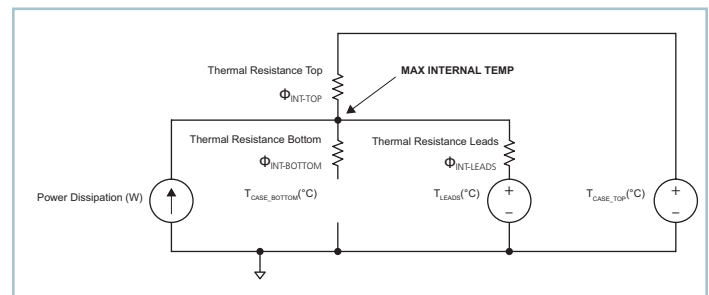


Figure 20 — Top case and leads thermal model

Figure 20 shows a scenario where there is no bottom side cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$$T_{INT} - PD_1 \cdot \Phi_{INT-TOP} = T_{CASE_TOP}$$

$$T_{INT} - PD_3 \cdot \Phi_{INT-LEADS} = T_{LEADS}$$

$$PD_{TOTAL} = PD_1 + PD_3$$

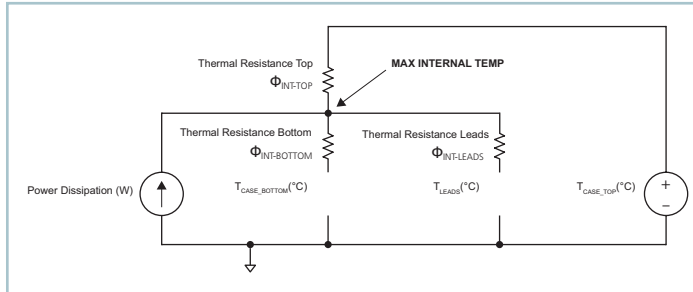


Figure 21 — Top case thermal model

Figure 21 shows a scenario where there is no bottom side and leads cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$$T_{INT} - PD_1 \cdot \Phi_{INT-TOP} = T_{CASE_TOP}$$

$$PD_{TOTAL} = PD_1$$

Please note that Vicor has a suite of online tools, including a simulator and thermal estimator which greatly simplify the task of determining whether or not a BCM thermal configuration is valid for a given condition. These tools can be found at: <http://www.vicorpower.com/powerbench>.

Current Sharing

The performance of the SACT™ topology is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- An input filter is required for an array of BCMs in order to prevent circulating currents.

For further details see [AN:016 Using BCM Bus Converters in High Power Arrays](#).

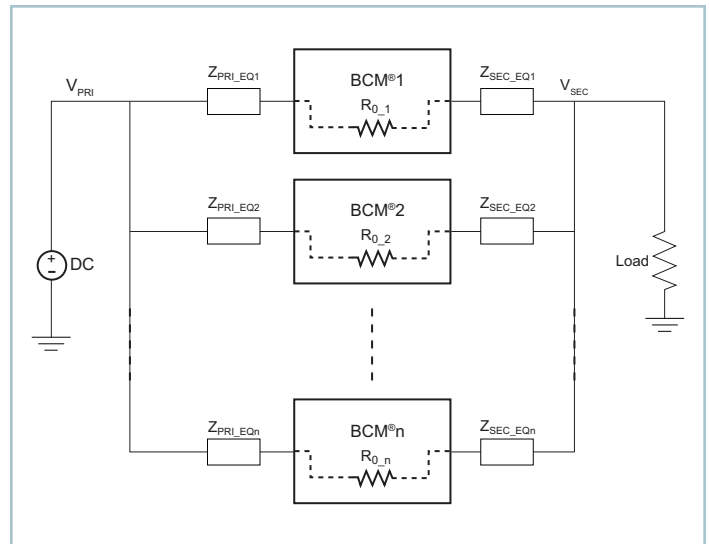


Figure 22 — BCM module array

Fuse Selection

In order to provide flexibility in configuring power systems VI Chip® modules are not internally fused. Input line fusing of VI Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

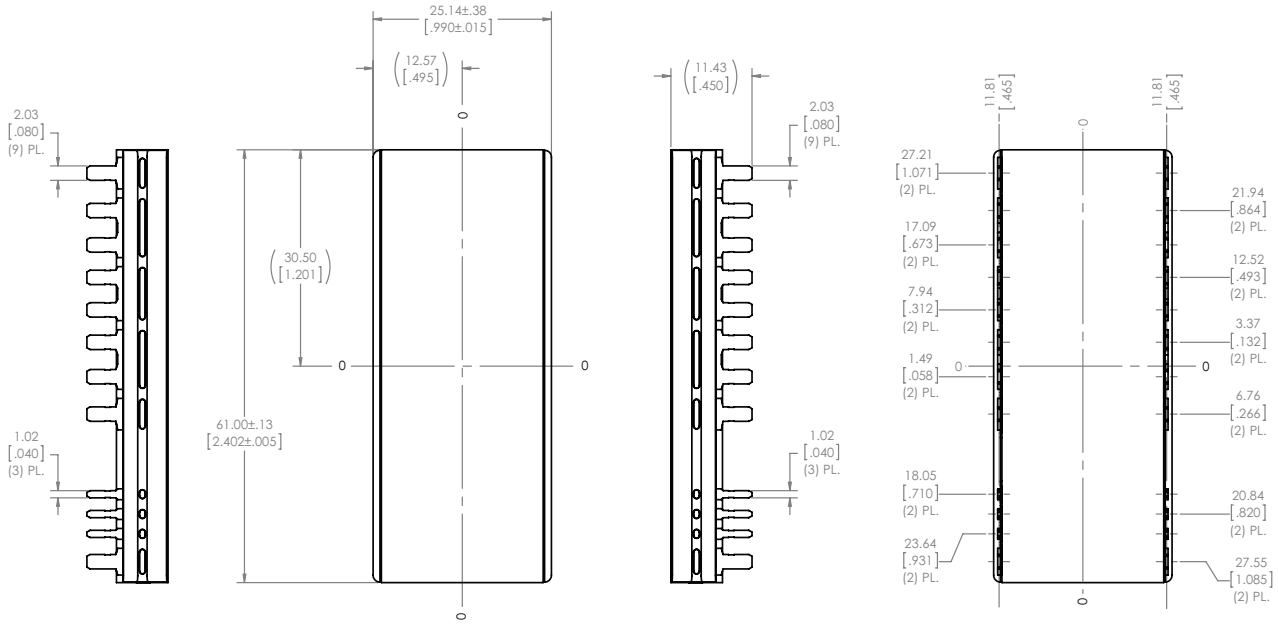
- Current rating (usually greater than maximum current of BCM module)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I²t
- Recommend fuse: ≤ 40A Littelfuse 456 Series (primary side)

Reverse Operation

BCM modules are capable of reverse power operation. Once the unit is started, energy will be transferred from secondary back to the primary whenever the secondary voltage exceeds V_{PRI} • K. The module will continue operation in this fashion for as long as no faults occur.

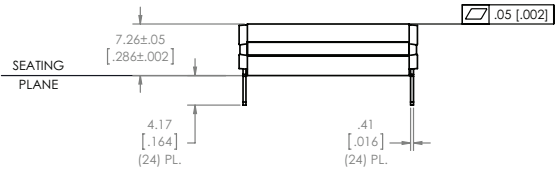
Transient operation in reverse is expected in cases where there is significant energy storage on the secondary and transient voltages appear on the primary.

BCM Module Through Hole Package Mechanical Drawing and Recommended Land Pattern

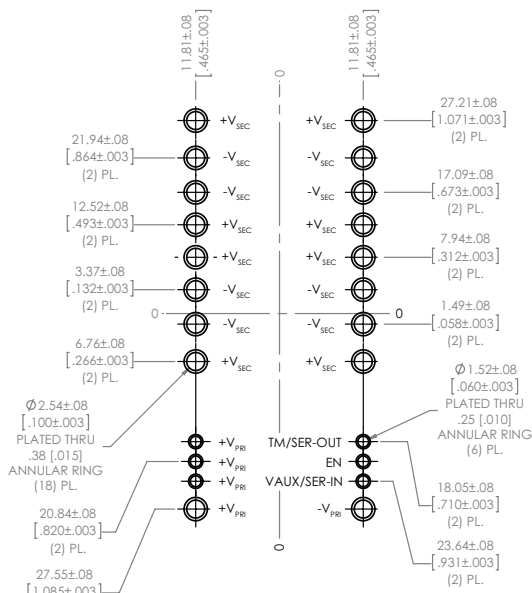


TOP VIEW (COMPONENT SIDE)

BOTTOM VIEW



NOTES:
 1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.
 2- UNLESS SPECIFIED OTHERWISE, DIMENSIONS ARE MM / [INCH], TOLERANCE ± 0.127 / [0.005]



RECOMMENDED HOLE PATTERN (COMPONENT SIDE)

Revision History

Revision	Date	Description	Page Number(s)
1.0	08/26/15	Initial Release	n/a
1.1	09/??/15	Changed PRI to SEC Input Quiescent Current	5
1.2	07/26/16	Added PMBus enabled product and associated related specifications Updated electrical specifications table for forward direction Added electrical specifications table for reverse direction Updated figure 2 Updated figures 14 & 15	all 5, 6 & 7 8 & 9 10 18

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