MitySOM-5CSx Design Guide

1 Overview

The MitySOM-5CSx family of modules are designed to take most of the pain out of developing a new product based on the Altera Cyclone V FPGAs that include ARM processing core[s]. The long list of requirements and costly board design specifications are handled by the module wherever possible. This, along with the board support package, makes it possible to quickly create new products with greatly reduced effort relative to creating a complete system design from scratch.

1.1 Fast Facts for Getting Started

Facts	MitySOM-5CSx
Required socket connector	MXM Connector, JAE MM70-314-310B1-1-R300 or equivalent
Input voltage Required	5V
Memory Peripherals (On Module)	EEPROM, QSPI NOR Flash, DDR3L SDRAM
On-Module HPS Peripherals[1]	USB_1, $UART_0$, I^2C_0
HPS Edge Peripherals[2]	$EMAC_1$, USB_0, $CAN_{0,1}$, MMC/SD/$SDIO_0$, $I^2C_{1,3}$, $SPIM_0$, and $SPIS_{0,1}$
HPS Fabric Peripherals[3]	$EMAC_{0,1}$, USB_0, $CAN_{0,1}$, $UART_1$, MMC/SD/$SDIO_0$, I^2C_2, and $SPIM_{0,1}$
Total number of FPGA I/Os	107 / 133
Differential I/Os	47 pairs / 60 pairs
Clock Differential I/Os	7 pairs
Exclusively Single Ended I/Os	7

The table above gives an idea of the peripherals and features available on the MitySOM. Additional details can be found in the list below with the HPS peripherals grouped by the FPGA Bank.

- **Bank7A** includes a mix of module peripherals and exposed HPS peripherals (**+3.3V**)
  - $UART_0$ Console Interface (by default in BSP)
  - I^2C_0 is used on the module for: EEPROM, RTC, Temperature Sensor, Debug LED Driver
  - TRACE Peripheral can be directed to the debug header or the edge connector
    - With the JTAG/TRACE adapter in TRACE Mode, the TRACE pins are used on the module
    - Under normal use, the TRACE pins (other peripherals) go to the edge connector as:
      - $SPIS_0$ / GPIOs
      - $SPIS_1$ / GPIOs / CAN_1
  - $SPIM_0$ / I^2C_1 / $UART_0$ Flow Control / CAN1 / GPIOs
  - CAN_0 / GPIOs
  - 25MHz HPS-CLK1 oscillator
  - HPS-CLK2 available through Edge Connector
  - HPS-PORSEL = Fast to support CvP
  - Reset I/O Connections – drive with open collector or open emitter
- **Bank7C** is exposed to the edge connector (**+3.3V** I/O) and supports:

[1] These HPS peripherals are on the module and must be chosen as the pin MUX option. The $UART_0$ pins are used by the console and are available on the Edge Connector – they are only supported at the default location.

[2] HPS Peripherals have very limited MUX options to choose the desired mix of peripherals. If an HPS peripheral choice blocks another desired peripheral, it can be accessed through the FPGA fabric. All these HPS Edge Pins can also be used for simple GPIO pins.

[3] These HPS peripherals can be accessed through the FPGA fabric and will consume some of the available I/O pins if used in this manner. If they are not listed as HPS Edge Peripherals[2], they can only be accessed through the FPGA fabric.

  - SDMMC x4 or x8
  - USB_0
  - GPIOs
- **Bank7B** and **Bank7D** share a common VIO (**+1.8V** to save power)
  - +VIO1.8V is provided by the module for the I/O supply
  - **Bank7B** uses the $QSPI_1$ peripheral for NOR flash on the SOM
  - **Bank7B** remaining pins go to the edge connector for other peripherals such as Ethernet
  - **Bank7D** uses the USB_1 peripheral, with the ULPI USB Phy on the SOM

There are three peripherals locked down on the MitySOM-5CSx. These were assigned to HPS peripheral locations while trying to maintain flexibility. The QSPI NOR Flash interface is only available in one location, and the included USB_1 peripheral was assigned to allow an external SDMMC interface. With those assigned, there are very few options for the required UART and I^2C peripherals. This leaves some serial peripherals and a mix of Ethernet, SD/MMC, NAND, USB, and GPIOs available for the end application to pick the desired mix.

1.2 MitySOM-5CSx Family Modules

The MitySOM-5CSx family of modules is available in a few configurations. These options provide a range of FPGA fabric and memory sizes to meet a range of applications. See the table below for a high level overview of the module configurations. More options may be available in the future, and additional options can be discussed with Critical Link if desired. The various module configurations are pin compatible. The initial range of module configurations is listed in Table 1. The I/O counts for each module configuration is listed in Table 2.

Table 1: MitySOM-5CSx Features

Feature	5CSE-L2-3YA	5CSE-H4-3YA	5CSX-H5-4YA	5CSX-H6-42A	5CSX-H6-53B
Temperature Range	C & I	I	I	C & I	C & I
ARM Cores / Speed	1 / 600MHz	2 / 800MHz	2 / 800MHz	2 / 800MHz	2 / 800MHz
Transceivers	0	0	6	6	6
FPGA Fabric	25kLE	40kLE	85kLE	110kLE	110kLE
FPGA DDR	0MB	0MB	0MB	256MB	512MB
HPS DDR	512MB	1GB+ECC	1GB+ECC	1GB+ECC	2GB+ECC
QSPI NOR Flash	16MB	16MB	32MB	32MB	48MB
EEPROM	16Kb	16kb	16kb	16kb	16kb
Temperature Sensor	✓	✓	✓	✓	✓
RTC	✓	✓	✓	✓	✓
RGB Debug LED	✓	✓	✓	✓	✓
Debug LED	Green	Green	Green	Green	Green
Power LED	Green	Green	Green	Green	Green
HPS CLK1	25MHz	25MHz	25MHz	25MHz	25MHz
CvP Supported			✓	✓	✓
FPP Config x16	✓ [4]	✓ [4]	✓ [4]		

[4]The additional pins required to support FPP are available on the module versions with expanded I/Os replacing the FPGA DDR connections.

[5]The FPGA DDR I/Os are on the module. The expanded I/O versions without FPGA DDR memory make 26 of these pins available on the edge connector.

Table 2: MitySOM-5CSx I/O Counts

I/O Counts	B3B	B4A	B0/1	B3A	B5A	B5B
5CSX-H6-42A						
GXB Pairs RX/TX/CLK			6/6/2			
FPGA IOs 3B	32					
FPGA IOs 4A		64				
PERST#					1	
FPGA DDR[5]				16	15	7
5CSX-H6-53B						
GXB Pairs			6/6/2			
FPGA IOs 3B	32					
FPGA IOs 4A		64				
PERST#					0	
FPGA DDR[5]				16	16	7
5CSE-L2-3YA						
GXB Pairs			0			
FPGA IOs 3B	32					
FPGA IOs 4A		64				
PERST#					1	
FPGA IOs 3A/5A/5B				16	10	0
5CSE-H4-3YA						
GXB Pairs			0			
FPGA IOs 3B	32					
FPGA IOs 4A		64				
PERST#					1	
FPGA IOs 3A/5A/5B				16	10	0
5CSX-H5-4YA						
GXB Pairs			6/6/2			
FPGA IOs 3B	32					
FPGA IOs 4A		64				
PERST#					1	
FPGA IOs 3A/5A/5B				16	10	0
5CSX-H6-4YA						
GXB Pairs			6/6/2			
FPGA IOs 3B	32					
FPGA IOs 4A		64				
PERST#					1	
FPGA IOs 3A/5A/5B				16	10	0

1.3 Module Dimensions

The MitySOM-5CSx modules measure 82mm x 39mm. A dimmensioned drawing of the module is shown in Figure 1. All dimensions shown are in milimeters.

1.4 Thermal Performance

Most designs will need some form of additional heatsink or active cooling to maintain the junction temperature within device limits. A fully loaded design will require significant cooling to operate reliably

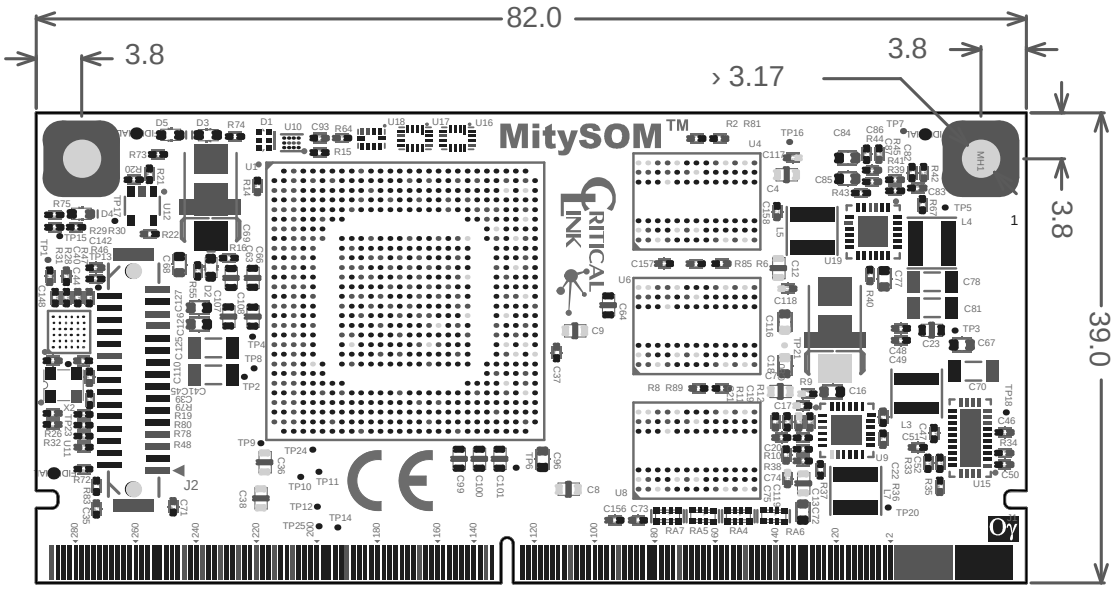

Figure 1: MitySOM-5CSx Mechanical Drawing

across the full commercial or industrial temperature range.

Designs that are not pushing the capabilities of the CycloneV and HPS performance can use various strategies to limit the power consumed. Some typical strategies to persue are running the HPS core clock frequency at a reduced rate. The MitySOM modules default to the 800MHz HPS operating frequency. Setting this to a slower clock rate will reduce the dynamic power consumption. The static power consumption is based on the leakage of the internal features and cannot be reduced easily.

When designing the FPGA logic, design choices play an important role in determining the power consumed. Faster clocks will consume more power proportional to the clock rate. Isolating the fast logic sections of a design and running logic slower where possible will provide a few benefits. Some of the benefits include reduced power consumption, and quicker compiles. At fast clock rates, the Quartus tools will have to work harder to meet timing. If the tools have difficuly in meeting timing, this will generally require longer design compiles. Altera has an application note, see AN:531[6] for additional details.

Fast I/O pins will also consume more power. If fast interfaces are desired, reduce the voltage standard where possible. Also reduce the capacitive load on the I/O connections in PCB layout. The dynamic power requirements increase linearly with the capacitance an I/O has to charge and discharge at each transition. The voltage is more significant because this term is expoenetial. The power required to drive an I/O pin is generally $P_{dyn} = 1/2CV^2f$. Checking various design scenarios is easily performed with the Early Power Estimator[7] and entering the I/O characteristics into the fields on the spreadsheet for each group of signals to get an estimate. As a design progresses, Quartus design details can be loaded into the EPE to get better estimates of power requirements.

Altera also has a Webcast[8] for getting an overview of power reductions on the 28nm devices, such as the Cyclone V used on the MitySOM-5CSx. The related White paper[9] can also be reviewed to get an

[6] http://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/an/an531.pdf
[7] https://www.altera.com/support/support-resources/devices/power/cy4-5-estimator.html
[8] http://www.altera.com/education/webcasts/all/wc-2010-lower-power-28nm.html
[9] http://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/wp/wp-01148-stxv-power-consumption.pdf

overview of the power saving features in the FPGA.

2 Connectors

2.1 MitySOM-5CSx Module Card Edge Pin-out

The MitySOM-5CSx uses the MXM standard connector for the edge connector interface. The module only uses the physical interface, and does not match the MXM electrical interface. Attempting to use the MitySOM in a MXM host is likely to damage one or both boards.

The MitySOM-5CSx family uses an MXM connector and general footprint with one exception – the double pin at the end has been separated into two individual pins numbered 278 and 280.

Note that the modules are NOT compatible with the MXM electrical standard... signal assignments, VIO voltages, etc. Intermixing modules/sockets from the two standards would very possibly cause permanent damage to one or both sides.

2.1.1 Top Edge Connector

At the end of the module are pins that are ganged together. These are ganged to match the MXM standard's[10] ganged pins. The first set of ganged pins is reserved for possible future high power modules.

Table 3: Top Edge Power

PIN	TYPE	SIGNAL	GROUP
E2	RSVD		Power
E2	RSVD		Power
E2	RSVD		Power
E2	RSVD		Power
E2	RSVD		Power
E2	RSVD		Power
E2	RSVD		Power
E2	RSVD		Power
E2	RSVD		Power
	GAP	NC	
	GAP	NC	
E4	PWR	GND	Power
E4	PWR	GND	Power
E4	PWR	GND	Power
E4	PWR	GND	Power
E4	PWR	GND	Power
E4	PWR	GND	Power
E4	PWR	GND	Power
E4	PWR	GND	Power
E4	PWR	GND	Power

[10] There is one difference between the ganged pins of the MXM specification and the MitySOM-5CSx's edge connector. At the high end of the connector in the MXM specification, there are two pins tied together. In the MitySOM these are separate pins numbered 278 and 280. The edge connector pins are uniformly spaced at 0.5mm pitch.

After the power pins, there is a group of HPS peripheral pins. These are generally used as serial interfaces, but are available as HPS GPIO pins as well. The default console serial interface is included here.

Table 4: Top Edge HPS Bank7A Peripheral I/O Pins

PIN	Ball	TYPE	SIGNAL	GROUP
2	B19	I	B7A_UART0_RX	Bank7A
4	C16	I/O	B7A_UART0_TX,CLKSEL0	Bank7A,CSEL
6	C17	I/O	B7A_UART0_RTS/SPIM0_MOSI/I2C1_SCL/HPS_GPIO58	Bank7A
8	A18	I/O	B7A_UART0_CTS/SPIM0_CLK/I2C1_SDA/HPS_GPIO57	Bank7A
10	H17	I/O	B7A_CAN0_TX,CLKSEL1/HPS_GPIO62	Bank7A,CSEL
12	A17	I/O	B7A_CAN0_RX/SPIM0_SS1/HPS_GPIO61	Bank7A
14	J17	I/O	B7A_CAN1_TX,BOOTSEL0/SPIM0_SS0/HPS_GPIO60	Bank7A,BSEL
16	B18	I/O	B7A_CAN1_RX/SPIM0_MISO/HPS_GPIO59	Bank7A
18	D7	PWR	VBAT+3V[11]	Power

On the MitySOM-5CSx, two of the simple serial interfaces are consumed. The main console UART is assigned by default to pins C16 and B19 for receive and transmit. There is generally no flow control required on the console interface. The I^2C_0 is consumed on the module to control a number of devices. This is assigned to pins B16 and C19 on the U23 package. The I^2C_0 interface controls the factory configuration EEPROM, the AB1803-T3 RTC, a LM73[12] temperature sensor, and the LP5562TMX debug LED driver to light the RGB LED and a green debug LED. The second UART peripheral, $UART_1$, could only be exposed on the pins consumed by the I^2C_0 interface. If the second UART is desired, it must be routed through the FPGA fabric.

The remaining Bank7A peripherals can be assigned as desired. The assignment options are listed in Table 5. If flow control is desired, it can be enabled for the console UART. Note that some of the Bank7A group of pins are also assigned to the BSEL and CSEL groups. The pins in the BSEL and CSEL groups are read at reset to identify the desired boot selection and clock divisor. The HPS_CLK1 is on the module and has a 25MHz oscillator – this is the reference clock during initial boot.

[11] The VBAT+3V input powers the RTC chip and V_{CCBAT} pin of the Cyclone V. If you do not use the design security feature in Cyclone V devices or need the RTC to maintain the time, connect to a 2.5V, or 3.0V power supply. The power-on reset (POR) circuitry monitors VCCBAT. Cyclone V devices do not exit POR if VCCBAT is not powered up.

[12] The original production version of the MitySOM-5CSX included a TC74A5 for the temperature sensor. Due to manufacturing fallout, the temperature sensor has been replaced with an LM73CIMK-1. These sensors reside at different I^2C addresses.

Table 5: Top Edge HPS Bank7A Peripheral Details

EDGE	BALL	TYPE	Description
2	B19	I	Console UART0 receive data
4	C16	O I	Console UART0 transmit data. CLKSEL0 value is read at reset, set with a pull-up or pull-down resistor of 1KΩ to 10KΩ
6	C17	O O I/O I/O	UART0_RTS – flow control is generally not required for the console UART. SPIM0_MOSI – SPI Master Data Out I^2C1_SCL HPS_GPIO58
8	A18	I O I/O I/O	UART0_CTS – flow control is generally not required for the console UART. SPIM0_CLK – SPI Master Clock I^2C1_SDA HPS_GPIO57
10	H17	O I I/O	CAN0_TX CLKSEL1 – value read at reset HPS_GPIO62
12	A17	I O I/O	CAN0_RX SPIM0_SS1 HPS_GPIO61
14	J17	O I O I/O	CAN1_TX BOOTSEL0 – value read at reset SPIM0_SS0 HPS_GPIO60
16	B18	I I I/O	CAN1_RX SPIM0_MISO HPS_GPIO59
18		PWR	Battery back-up power supply (For RTC and design security volatile key register)

Table 6: Top Edge HPS Bank7A MUXed Debug Peripheral I/O Pins

PIN	Ball	TYPE	SIGNAL	GROUP
20	C18	I/O	B7A_TRACE_D7/SPIS1_MISO/HPS_GPIO56	Bank7A-MUXed
22	A19	I/O	B7A_TRACE_D6/SPIS1_SS0/HPS_GPIO55	Bank7A-MUXed
24	J18	I/O	B7A_TRACE_D5/SPIS1_MOSI/CAN1_TX/HPS_GPIO54	Bank7A-MUXed
26	A20	I/O	B7A_TRACE_D4/SPIS1_CLK/CAN1_RX/HPS_GPIO53	Bank7A-MUXed
28	K18	I/O	B7A_TRACE_D3/SPIS0_SS0/HPS_GPIO52	Bank7A-MUXed
30	A21	I/O	B7A_TRACE_D2/SPIS0_MISO/HPS_GPIO51	Bank7A-MUXed
32	B21	I/O	B7A_TRACE_D1/SPIS0_MOSI/HPS_GPIO50	Bank7A-MUXed
34	A22	I/O	B7A_TRACE_D0/SPIS0_CLK/HPS_GPIO49	Bank7A-MUXed
36	K9	I	B9A_MSEL4	MSEL
38	C21	I	B7A_TRACE_CLK/HPS_GPIO_48	Bank7A-MUXed
40		PWR	GND	Power

The Bank7A-MUXed group of signals includes the TRACE[13] peripheral. This group will generally provide the most benefit for debug or some additional GPIO pins. The debug connector on the MitySOM module provides a means to have the TRACE peripheral routed to the debug peripheral instead of the edge connector when the debug adapter is connected. This eliminates the need to include the Mictor TRACE connector on the carrier board merely to support debug efforts. The debug board can operate in JTAG-chain mode and leave the Bank7A-MUXed pins routed to the edge connector, or be manually set into the TRACE debug mode and route the TRACE connections to the Mictor TRACE connector on the debug adapter.

The TRACE peripheral pins are routed through bidirectional analog MUXes on the MitySOM. These are fast enough to support the maximum speed of the SPI Slave peripherals that could be assigned to those pins, running as fast as 50MHz or the GPIOs, which have a minimum detectable pulse width of 2us, based on a debounce clock frequency of 1MHz. The CAN peripheral has a maximum data rate of 1Mbps, and the I^2C interfaces top out at 500KHz.

Table 7: Top Edge HPS Bank7A-MUXed Peripheral Details

PIN	Ball	TYPE	Description
20	C18	O	TRACE_D7
		O	SPIS1_MISO – SPI Slave Data Output
		I/O	HPS_GPIO56
22	A19	O	TRACE_D6
		I	SPIS1_SS0 – SPI Slave Select
		I/O	HPS_GPIO55
24	J18	O	TRACE_D5
		I	SPIS1_MOSI – SPI Slave Data Input
		O	CAN1_TX
		I/O	HPS_GPIO54
26	A20	O	TRACE_D4
		I	SPIS1_CLK – SPI Slave Clock Input
		I	CAN1_RX
		I/O	HPS_GPIO53
28	K18	O	TRACE_D3
		I	SPIS0_SS0 – SPI Slave Select Input
		I/O	I2C1_SCL
		I/O	HPS_GPIO52
30	A21	O	TRACE_D2
		O	SPIS0_MISO – SPI Slave Data Output
		I/O	HPS_GPIO51
		I/O	I2C1_SDA
32	B21	O	TRACE_D1
		I	SPIS0_MOSI – SPI Slave Data Input
		I/O	HPS_GPIO50
34	A22	O	TRACE_D0
		I	SPIS0_CLK – SPI Slave Clock Input
		I/O	HPS_GPIO49
36	K9	I	MSEL4 – value read at power-on
38	C21	O	TRACE_CLK – Trace Clock Output
		I/O	HPS_GPIO48

[13] http://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/cyclone-v/cv_54007.pdf CoreSight Debug and Trace. Note that TRACE can be run over JTAG as well.

Table 8: Top Edge Bank5A Expanded I/O Pins

PIN	BALL	TYPE	SIGNAL	GROUP
42	AC24	I/O	NC,B5A_TX_R5_P/DEV_OE	NC,Bank5A
44	AB23	I/O	NC,B5A_TX_R5_N/DEV_CLR_N	NC,Bank5A

The general FPGA I/O pins are assigned signal names based on the 110KLE Cyclone V device. They are also assigned signal names according to the highest achievable performance. For each differential pair, there is a SERDES block in hard IP that can operate in a single direction. To make use of the greatest level of performance on these I/Os, connect the Bank4A pairs as transmit pairs using the SERDES blocks.

These pins can all be used as input pins, output pins, or bidirectional pins if the SERDES block is not required. Many of the signals can also operate as Emulated LVDS Output channels, but note that some of the signals do not have a complete pair. On the U23 package used on the MitySOM, not all the signals are paired up, such as B76_N and B57_P. Many of these pins can also be used for various DDR memory interfaces and connect to the Hard Memory Controller. Please refer to the Altera pin assignment spreadsheet for these assignment options. The FPGA used on the MitySOM-5CSx is the U23 package with 672 pins.

The smaller MitySOM-5CSE does not include the Hard Memory Controller. It also gives up the seven pins of Bank5B that are used by the FPGA DDR interface on the MitySOM. Other than that and the obviously missing high speed transceivers, the designs can migrate to larger or smaller options as desired. Note that the pin assignments remain the same on the smaller devices, size A2 to A4, but the signal names and pair numbering is not the same. The larger size 5 and 6 FPGAs use the signal name assignments detailed in the MitySOM design documents.

One of the Bank4A pins, pin AH7 can also be used for the termination resistor reference current. If using an I/O standard that requires calibrated on-chip terminations, connect the required resistor to the RZQ pin. If using a MitySOM-5CSx with the FPGA DDR memory, there is an RZQ reference with a 240Ω resistor on pin AB25. In some designs this RZQ reference connection can be shared.

[14]The VREF4AN0 is half the externally supplied VIO_4A voltage.

Table 9: Top Edge FPGA Bank4A I/O Pins

PIN	Ball	TYPE	SIGNAL	GROUP
46		PWR	GND	Power
48		PWR	+VIO_4A [14]	Power
50		PWR	GND	Power
52	AF27	I/O	B4A_TX_B80_P	Bank4A
54	AF28	I/O	B4A_TX_B80_N	Bank4A
56	AG28	I/O	B4A_TX_B77_P	Bank4A
58	AH27	I/O	B4A_TX_B77_N	Bank4A
60	AH26	I/O	B4A_TX_B76_N	Bank4A
62	AG26	I/O	B4A_TX_B73_P	Bank4A
64	AG24	I/O	B4A_TX_B72_P	Bank4A
66	AH24	I/O	B4A_TX_B72_N	Bank4A
68	AH23	I/O	B4A_TX_B69_P	Bank4A
70	AH22	I/O	B4A_TX_B69_N	Bank4A
72		PWR	GND	Power
74	AH21	I/O	B4A_TX_B68_N	Bank4A
76	AG21	I/O	B4A_TX_B65_P	Bank4A
78	AF20	I/O	B4A_TX_B64_P	Bank4A
80	AG20	I/O	B4A_TX_B64_N	Bank4A
82	AG19	I/O	B4A_TX_B61_P	Bank4A
84	AH19	I/O	B4A_TX_B61_N	Bank4A
86	AG18	I/O	B4A_TX_B60_P	Bank4A
88	AH18	I/O	B4A_TX_B60_N	Bank4A
90	AF18	I/O	B4A_TX_B57_P	Bank4A
92		PWR	GND	Power
94	AH17	I/O	B4A_TX_B56_P	Bank4A
96	AH16	I/O	B4A_TX_B56_N	Bank4A
98	AG15	I/O	B4A_TX_B53_P	Bank4A
100	AH14	I/O	B4A_TX_B53_N	Bank4A
102	AG14	I/O	B4A_TX_B52_P	Bank4A
104	AH13	I/O	B4A_TX_B52_N	Bank4A
106	AH12	I/O	B4A_TX_B49_P	Bank4A
108		PWR	GND	Power
110	AG11	I/O	B4A_TX_B48_P	Bank4A
112	AH11	I/O	B4A_TX_B48_N	Bank4A
114	AG10	I/O	B4A_TX_B45_P	Bank4A
116	AH9	I/O	B4A_TX_B45_N	Bank4A
118	AG9	I/O	B4A_TX_B44_P	Bank4A
120	AH8	I/O	B4A_TX_B44_N	Bank4A
122	AG8	I/O	B4A_TX_B41_P	Bank4A
124	AH7	I/O	B4A_TX_B41_N/RZQ0	Bank4A

Table 10: Top Edge Key Missing Pins

PIN	TYPE	SIGNAL	GROUP
126	KEY	—	
128	KEY	—	
130	KEY	—	
132	KEY	—	

Bank3B signals are another group of general FPGA I/O pins. These should be treated the same as the Bank4A pins. Additionally, there is a pair of connections that have dedicated clock routes to the Bottom Left Fractional PLL. If the fPLL external feedback is needed, or the CLKOUT from the fPLL, be sure to properly assign these resources.

Table 11: Top Edge FPGA Bank3B I/O Pins

PIN	Ball	TYPE	SIGNAL	GROUP
134		PWR	+VIO_3B [15]	Power
136		PWR	GND	Power
138	AE8	I/O	B3B_TX_B29_P	Bank3B
140	AF9	I/O	B3B_TX_B29_N	Bank3B
142	AE7	I/O	B3B_TX_B28_P	Bank3B
144	AF8	I/O	B3B_TX_B28_N	Bank3B
146	AF5	I/O	B3B_TX_B32_P	Bank3B
148	AF6	I/O	B3B_TX_B32_N	Bank3B
150	AF7	I/O	B3B_TX_B33_P	Bank3B
152	AG6	I/O	B3B_TX_B33_N	Bank3B
154	AH6	I/O	B3B_TX_B40_P	Bank3B
156	AH5	I/O	B3B_TX_B40_N	Bank3B
158		PWR	GND	Power
160	AG5	I/O	B3B_TX_B37_P/BL_CLKOUT0/BL_CLKOUT_P/FPLL_BL_FB	Bank3B
162	AH4	I/O	B3B_TX_B37_N/BL_CLKOUT1/BL_CLKOUT_N	Bank3B
164	AE4	I/O	B3B_TX_B25_P	Bank3B
166	AF4	I/O	B3B_TX_B25_N	Bank3B
168	AH3	I/O	B3B_TX_B36_P	Bank3B
170	AH2	I/O	B3B_TX_B36_N	Bank3B

Bank8A provides a few clock connection to the Top Left Fractional PLL. Note that there may be difficulty routing this clear across the FPGA to use with logic in the quadrants that include the Bank3 and Bank4 I/O pins.

Table 12: Top Edge FPGA Bank8A I/O Pins

PIN	Ball	TYPE	SIGNAL	GROUP
172	E11	I/O	CLK6_P/FPLL_TL_FB_P/B8A_RX_T9_P	Bank8A
174	D11	I/O	CLK6_N/FPLL_TL_FB_N/B8A_RX_T9_N	Bank8A
176		PWR	VIO_8A [16]	Power
178	E8	I/O	TL_CLKOUT0/TL_CLKOUT_P/FPLL_TL_FB/B8A_TX_T4_P	Bank8A
180	D8	I/O	TL_CLKOUT1/TL_CLKOUT_N/B8A_TX_T4_N	Bank8A
182		PWR	GND	Power

Before the high speed transceiver interface pins there is a group of reserved edge connector pins. These are reserved for a version of the module with expanded I/O connections replacing the FPGA DDR memory interface on the original MitySOM-5CSX. The FPGA DDR memory is connected to Banks 3A, 5A, and 5B. With the memory removed, there are pins available for most of the Bank3A and Bank5A connections. These pins also provide access to the fast parallel configuration options available in the Cyclone V. If these features are desired in an ed application, please contact Critical Link and inquire about availability.

[15] The VREF3BN0 is half the externally supplied VIO_3B voltage.
[16] The VREF8AN0 is half the externally supplied VIO_8A voltage.

Table 13: Top Edge FPGA Bank3A Expanded I/O Pins

PIN	Ball	TYPE	SIGNAL [17]	GROUP
184	AD5	I/O	NC,B3A_TX_B8_P	NC,Bank3A
186	AE6	I/O	NC,B3A_TX_B8_N/PR_READY	NC,Bank3A
188	AC4	I/O	NC,B3A_TX_B6_P/DATA15	NC,Bank3A
190	AD4	I/O	NC,B3A_TX_B6_N/DATA13	NC,Bank3A
192	AA4	I/O	NC,B3A_TX_B4_P/DATA11	NC,Bank3A
194	AB4	I/O	NC,B3A_TX_B4_N/DATA9	NC,Bank3A
196	Y5	I/O	NC,B3A_TX_B2_P/DATA7	NC,Bank3A
198	Y4	I/O	NC,B3A_TX_B2_N/DATA5	NC,Bank3A

The MitySOM-5CSX[18] includes 6 channels of high speed transceivers. These are available in groups of 3 transceivers and a reference clock. The receive pairs are available on the top edge of the module. The PCI Express Hard Controller can also be utilized through these transceivers. If using the PCIe interface, it is recommended to assign the channels starting with pair 0 along with the GXB_REFCLK0 pair. The PCIe can be configured as an endpoint or a root port. As an endpoint, the Configuration via Protocol (CvP) can be utilized for the fastest configuration option.

Table 14: Top Edge High Speed Transceiver Pins

PIN	Ball	TYPE	SIGNAL [18]	GROUP
200		PWR	GND	Power
202	AF2	I	GXB_RX_0_P,NC	GXB0,NC
204	AF1	I	GXB_RX_0_N,NC	GXB0,NC
206		PWR	GND	Power
208	AB2	I	GXB_RX_1_P,NC	GXB0,NC
210	AB1	I	GXB_RX_1_N,NC	GXB0,NC
212		PWR	GND	Power
214	V2	I	GXB_RX_2_P,NC	GXB0,NC
216	V1	I	GXB_RX_2_N,NC	GXB0,NC
218		PWR	GND	Power
220	V5	I	GXB_REFCLK0_P,NC	GXB0,NC
222	V4	I	GXB_REFCLK0_N,NC	GXB0,NC
224		PWR	GND	Power
226	P2	I	GXB_RX_3_P,NC	GXB1,NC
228	P1	I	GXB_RX_3_N,NC	GXB1,NC
230		PWR	GND	Power
232	K2	I	GXB_RX_4_P,NC	GXB1,NC
234	K1	I	GXB_RX_4_N,NC	GXB1,NC
236		PWR	GND	Power
238	F2	I	GXB_RX_5_P,NC	GXB1,NC
240	F1	I	GXB_RX_5_N,NC	GXB1,NC

The last group of signals provide additional HPS peripheral connections. As shown in Table 15, the Bank7C peripherals are available here. These connections provide access to the SD/MMC peripheral

[17] These pins are reserved for modules that include the FPGA DDR interface. They are available on modules with Expanded I/O. Some of the expanded I/O pins can also be used for a wide configuration interface.

[18] The MitySOM-5CSE does not include the high speed transceivers on the FPGA. The GXB_RX pins should be pulled low through a 10KΩ resistor to ground as noted in the Quartus pin report for 5CSE support.

or the USB0 peripheral. The USB1 group of signals are assigned to the peripheral on Bank7D. The MitySOM includes a USB ULPI Phy, the TUSB1211A1 from Texas Instruments, and the USB interface is provided through the edge connector pins. This provides the USB interface while consuming the minimal amount of pins. This USB interface includes the connections necessary to run the USB port in host mode or on-the-go. To complete the interface, add the USB_VBUS power switch as desired, the required bulk capacitance, ESD protection, and the USB connector.

Table 15: Top Edge Bank7C and Bank7D Peripheral I/O Pins

PIN	Ball	TYPE	SIGNAL	GROUP
242		I^{PU}	USB1_FAULT_N	USB1
244	B12	I/O	SDMMC_CLK_IN/USB0_CLK/HPS_GPIO44	Bank7C
246		O^{PU}	USB1_PS_ON	USB1
248	B6	I/O	SDMMC_D1/USB0_D3/HPS_GPIO39	Bank7C
250	C13	I/O	SDMMC_D0/USB0_D2/HPS_GPIO38	Bank7C
252	A5	I/O	SDMMC_PWREN/USB0_D1/HPS_GPIO37	Bank7C
254	B8	I/O	SDMMC_CLK/USB0_STP/HPS_GPIO45	Bank7C
256		O	RTC_PSW/IRQ2_N [19]	RTC
258	D14	I/O	SDMMC_CMD/USB0_D0/HPS_GPIO36	Bank7C
260	B9	I/O	SDMMC_D3/USB0_NXT/HPS_GPIO47	Bank7C
262	B11	I/O	SDMMC_D2/USB0_DIR/HPS_GPIO46	Bank7C
264	H13	I/O	SDMMC_D4/USB0_D4/HPS_GPIO40	Bank7C
266	A4	I/O	SDMMC_D5/USB0_D5/HPS_GPIO41	Bank7C
268	H12	I/O	SDMMC_D6/USB0_D6/HPS_GPIO42	Bank7C
270	B4	I/O	SDMMC_D7/USB0_D7/HPS_GPIO43	Bank7C
272		I/O	USB1_ID	USB1
274		I/O	USB1_D_N	USB1
276		I/O	USB1_D_P	USB1
278		PWR[20]	+USB1_VBUS [21]	USB1
280		PWR	GND	Power

2.1.2 Bottom Edge Connector

On the bottom edge connector, the first group of signals include a mix of configuration signals and various reset/control signals. The MSEL pins define the FPGA configuration mode. Altera recommends tying the MSEL connections directly to power or ground. If configuring the FPGA from the HPS, set the MSEL to one of the FPPx16[22] configuration options. For many designs, this can simply be set to MSEL=00000. Note that there are 5 MSEL connections – one is on the top edge connector.

The Config group of pins provides the connections necessary to configure the FPGA from a prom. The MitySOM-5CSx Dev Board includes a footprint to solder in a prom to try this interface out. The expanded I/O versions of the MitySOM-5CSx support wider configuration interfaces.

[19] The RTC_PSW/IRQ2_N output is an output from the AB1805-T3 real-time clock. This can be used for a periodic power-up or other creative power saving modes. See *3.2 VCC Power Switched* section of the Abracon AB1805-T3 datasheet for details of switched power.

[20] This net includes a 0.1uF cap. Add the bulk capacitance necessary to meet the USB specification for your device application. This will generally be 1uF to 100uF and is specific to the mode of operation for the USB endpoint.

[21] Connect a 1KΩ series resistor to +5V_USB_VBUS to avoid the danger of a possible connection to the adjacent GND pin. The module only needs to sample the USB1_VBUS voltage for controlling the USB phy to support Ont-th-Go operation.

[22] https://www.altera.com/en_US/pdfs/literature/hb/cyclone-v/cv_52007.pdf There are many configuration options for the Cyclone V such as the configuration mode, bitstream compression, design security. The details can be found in Altera's dosumentation.

Table 16: Bottom Edge Reserved [High] Power Pins

PIN	TYPE	SIGNAL	GROUP
E1	PWR	RSVD	
E1	PWR	RSVD	
E1	PWR	RSVD	
E1	PWR	RSVD	
E1	PWR	RSVD	
E1	PWR	RSVD	
E1	PWR	RSVD	
E1	PWR	RSVD	
E1	PWR	RSVD	
	GAP	NC	
	GAP	NC	
E3	PWR	GND	Power
E3	PWR	GND	Power
E3	PWR	GND	Power
E3	PWR	GND	Power
E3	PWR	GND	Power
E3	PWR	GND	Power
E3	PWR	GND	Power
E3	PWR	GND	Power
E3	PWR	GND	Power

Table 17: Bottom Edge Main Power Pins

PIN	TYPE	SIGNAL	GROUP
1	PWR	VIN+5V	Power
3	PWR	VIN+5V	Power
5	PWR	VIN+5V	Power
7	PWR	VIN+5V	Power
9	PWR	VIN+5V	Power
11	PWR	GND	Power
13	PWR	GND	Power
15	PWR	GND	Power
17	PWR	GND	Power

Both reset connections are available on the edge connector: hard and soft reset; also known as cold and warm reset. The hard reset is the Power-On-Reset (POR) and is active low. The soft reset is labeled HPS_RST_N. These should be connected to an open collector output if driving the reset from the carrier board. The MitySOM module includes a 10KΩ pull-up resistor on each reset line. The lone Bank5A connection is here to provide the PCIe reset connection required to support CvP configuration. This signal is on a 1.35V bank, but can be pulled to +3.3V with a 10KΩ resistor. If not using this signal for the PCIe interface, it can be used as an additional FPGA I/O.

The Bank7A HPS_CLK2 connection is available here as well. This can be used to run the HPS peripherals off a clock source other than the 25MHz included on the MitySOM. This is not required in many designs. Additionally, two pairs of connections are reserved here for Expanded I/O versions. On modules without Expanded I/O, these pins are not connected.

[23]These signals are only available on the modules with expanded I/O; otherwise, they are not connected internal to the module.

Table 18: Bottom Edge Config Group Pins

PIN	Ball	TYPE	SIGNAL	GROUP
19	D20	I	B7A_HPS_CLK2	Bank7A
21	W15	I/O	B5A_PERSTL1_N	Bank5A
23	A23	I/O^{PU10K}	HPS_RST_N	Reset
25	H19	I/O^{PU10K}	HPS_POR_N	Reset
27	AA8	I/O	PGM_FPGA_DCLK	Config
29	J10	I	B9A_MSEL0	MSEL
31	AB6	I/O	PGM_FPGA_D3	Config
33	AC5	I/O	PGM_FPGA_D2	Config
35	AC6	I/O	PGM_FPGA_D1	Config
37	AD7	I/O	PGM_FPGA_D0	Config
39	F7	I/O^{PU10K}	B9A_nCONFIG	Config
41	H8	I/O^{PU10K}	B9A_nSTATUS	Config
43	AA6	I/O	PGM_FPGA_CSO_N	Config
45	H9	I	B9A_MSEL1	MSEL
47	AF26	I/O	NC,B5A_TX_R1_P [23]	NC,Bank5A
49	AE26	I/O	NC,B5A_TX_R1_N/PR_REQUEST [23]	NC,Bank5A
51	G6	I	B9A_MSEL2	MSEL
53	AE25	I/O	NC,B5A_TX_R3_P/nCEO [23]	NC,Bank5A
55	AD26	I/O	NC,B5A_TX_R3_N/CvP_CONFDONE [23]	NC,Bank5A
57	K10	I	B9A_MSEL3	MSEL

Table 19 shows the Bank4A connections available on the bottom edge connector. These are similar to the Bank4A connections on the top edge, but include receive SERDES Hard IP blocks. These can also be used as Emulated LVDS outputs and the signal names are assigned based on the 110KLE device connections. There are two clock input pairs in this group as well. The CLK2 pair is labeled CLK2DDR because the clock reference for the FPGA DDR interface should be brought in on this pair. This is necessary to meet timing for the FPGA DDR interface. If this clock source is a single ended signal, preference should be given to the CLK2DDR_P input because this input pin has a dedicated input to the fPLL and will have the best jitter performance.

There is a key slot for edge connector alignment. Table 20 identifies the missing pins.

Two more Bank4A pairs are available after the key slot. Then there is a group of Bank3B pairs and a Bank8A pair. Two of the pairs in this group are clock inputs. CLK0 also has the external feedback connection for the Bottom Left fPLL.

Table 19: Bottom Edge Bank4A I/O Pins

PIN	Ball	TYPE	SIGNAL	GROUP
59		PWR	GND	Power
61	AF25	I/O	B4A_RX_B78_P	Bank4A
63	AG25	I/O	B4A_RX_B78_N	Bank4A
65	AC22	I/O	B4A_RX_B75_P	Bank4A
67	AC23	I/O	B4A_RX_B75_N	Bank4A
69	AE24	I/O	B4A_RX_B74_P	Bank4A
71	AE23	I/O	B4A_RX_B74_N	Bank4A
73	AG23	I/O	B4A_RX_B70_P	Bank4A
75	AF23	I/O	B4A_RX_B70_N	Bank4A
77	AD23	I/O	B4A_RX_B67_P	Bank4A
79	AE23	I/O	B4A_RX_B67_N	Bank4A
81		PWR	GND	Power
83	AF22	I/O	B4A_RX_B66_P	Bank4A
85	AF21	I/O	B4A_RX_B66_N	Bank4A
87	AE20	I/O	B4A_RX_B62_P	Bank4A
89	AD20	I/O	B4A_RX_B62_N	Bank4A
91	AA19	I/O	B4A_RX_B59_P	Bank4A
93	AA18	I/O	B4A_RX_B59_N	Bank4A
95	AE19	I/O	B4A_RX_B58_P	Bank4A
97	AD19	I/O	B4A_RX_B58_N	Bank4A
99	Y15	I/O	B4A_RX_B55_P/CLK3_P	Bank4A
101	AA15	I/O	B4A_RX_B55_N/CLK3_N	Bank4A
103		PWR	GND	Power
105	AD17	I/O	B4A_RX_B54_P	Bank4A
107	AE17	I/O	B4A_RX_B54_N	Bank4A
109	W14	I/O	B4A_RX_B51_P	Bank4A
111	V13	I/O	B4A_RX_B51_N	Bank4A
113	AF17	I/O	B4A_RX_B50_P	Bank4A
115	AG16	I/O	B4A_RX_B50_N	Bank4A
117	Y13	I/O	CLK2DDR_P/B4A_RX_B47_P	Bank4A
119	AA13	I/O	CLK2DDR_N/B4A_RX_B47_N	Bank4A
121	AF15	I/O	B4A_RX_B46_P	Bank4A
123	AE15	I/O	B4A_RX_B46_N	Bank4A
125		PWR	GND	Power

Table 20: Bottom Edge Key Missing Pins

PIN	TYPE	SIGNAL	GROUP
127	KEY	—	
129	KEY	—	
131	KEY	—	

Table 21: Bottom Edge Bank4A & Bank3B I/O Pins

PIN	Ball	TYPE	SIGNAL	GROUP
133	U14	I/O	B4A_RX_B43_P	Bank4A
135	U13	I/O	B4A_RX_B43_N	Bank4A
137	AG13	I/O	B4A_RX_B42_P	Bank4A
139	AF13	I/O	B4A_RX_B42_N	Bank4A
141	AE12	I/O	B3B_RX_B38_P	Bank3B
143	AD12	I/O	B3B_RX_B38_N	Bank3B
145	AD11	I/O	B3B_RX_B30_P	Bank3B
147	AE11	I/O	B3B_RX_B30_N	Bank3B
149	AF11	I/O	B3B_RX_B34_P	Bank3B
151	AF10	I/O	B3B_RX_B34_N	Bank3B
153		PWR	GND	Power
155	T13	I/O	B3B_RX_B35_P	Bank3B
157	T12	I/O	B3B_RX_B35_N	Bank3B
159	T11	I/O	B3B_RX_B27_P	Bank3B
161	U11	I/O	B3B_RX_B27_N	Bank3B
163	V12	I/O	B3B_RX_B39_P	Bank3B
165	W12	I/O	B3B_RX_B39_N	Bank3B
167	V11	I/O	B3B_RX_B31_P/CLK0_P/FPLL_BL_FB_P	Bank3B
169	W11	I/O	B3B_RX_B31_N/CLK0_N/FPLL_BL_FB_N	Bank3B
171	AD10	I/O	B3B_RX_B26_P	Bank3B
173	AE9	I/O	B3B_RX_B26_N	Bank3B
175		PWR	GND	Power
177	D12	I/O	B8A_RX_T1_P/CLK7_P	Bank8A
179	C12	I/O	B8A_RX_T1_N/CLK7_N	Bank8A

On the bottom, there is another group of reserved edge connector pins before the high speed transceiver connections. Table 22 has the details of these Expanded I/O connections. On the expanded I/O version of the module, there is an additional VIO power input to power the FPGA banks consumed by the FPGA DDR memory interface on the original module. This is currently a no-connect. Carrier board designs that expect to migrate to the smaller MitySOM-5CSE device should provide power to this pin.

Table 22: Bottom Edge Bank5A/3A Expanded I/O Pins

PIN	Ball	TYPE	SIGNAL	GROUP
181		PWR	NC,+VIO_3A5A5B	Expanded I/O
183	AA20	I/O	NC,B5A_RX_R2_P	NC,Bank5A
185	Y19	I/O	NC,B5A_RX_R2_N	NC,Bank5A
187	Y17	I/O	NC,B5A_RX_R4_P	NC,Bank5A
189	Y18	I/O	NC,B5A_RX_R4_N	NC,Bank5A
191	Y11	I/O	NC,B3A_RX_B7_P	NC,Bank3A
193	AA11	I/O	NC,B3A_RX_B7_N	NC,Bank3A
195	U10	I/O	NC,B3A_RX_B5_P	NC,Bank3A
197	V10	I/O	NC,B3A_RX_B5_N	NC,Bank3A
199	U9	I/O	NC,B3A_RX_B3_P	NC,Bank3A
201	T8	I/O	NC,B3A_RX_B3_N	NC,Bank3A
203	W8	I/O	NC,B3A_RX_B1_P	NC,Bank3A
205	Y8	I/O	NC,B3A_RX_B1_N	NC,Bank3A

The transmit interfaces of the high speed transceivers are available on the bottom edge connector along with the second reference clock input. These connections are detailed in Table 23.

Table 23: Bottom Edge High Speed Transceiver Pins

PIN	Ball	TYPE	SIGNAL	GROUP
207		PWR	GND	Power
209	AD2	O	GXB_TX_0_P	GXB0
211	AD1	O	GXB_TX_0_N	GXB0
213		PWR	GND	Power
215	Y2	O	GXB_TX_1_P	GXB0
217	Y1	O	GXB_TX_1_N	GXB0
219		PWR	GND	Power
221	T2	O	GXB_TX_2_P	GXB0
223	T1	O	GXB_TX_2_N	GXB0
225		PWR	GND	Power
227	P8	I	GXB_REFCLK1_P	GXB1
229	N8	I	GXB_REFCLK1_N	GXB1
231		PWR	GND	Power
233	M2	O	GXB_TX_3_P	GXB1
235	M1	O	GXB_TX_3_N	GXB1
237		PWR	GND	Power
239	H2	O	GXB_TX_4_P	GXB1
241	H1	O	GXB_TX_4_N	GXB1
243		PWR	GND	Power
245	D2	O	GXB_TX_5_P	GXB1
247	D1	O	GXB_TX_5_N	GXB1

The last group of signals are the connections to Bank7B. These connections could be an RGMII Ethernet phy interface, an interface to NAND or more GPIO connections. The I/O voltage rail power for this interface is provided by the MitySOM and is +1.8V. This I/O voltage was chosen to save some power. Unfortunately, this limits the available NAND densities available as well as the maximum size of the QSPI device on the MitySOM. If an application requires much larger flash memory, please contact Critical Link to discuss the application.

Table 24: Bottom Edge Bank7B I/O Pins

PIN	Ball	TYPE	SIGNAL	GROUP
249		PWR	RES_BOOTSEL1 [24]	BSEL
251	J12	I/O	RGMII1_RX_CLK/NAND_DQ5/HPS_GPIO24	Bank7B
253	D15	I/O	HPS_GPIO28,BOOTSEL2/NAND_WE	Bank7B,BSEL
255	J13	I/O	RGMII1_RX_CTL/NAND_DQ3/HPS_GPIO22	Bank7B
257	A14	I/O	RGMII1_RXD0/NAND_DQ0/HPS_GPIO19	Bank7B
259	A11	I/O	RGMII1_RXD1/NAND_DQ6/HPS_GPIO25	Bank7B
261	C15	I/O	RGMII1_RXD2/NAND_DQ7/HPS_GPIO26	Bank7B
263	A9	I/O	RGMII1_RXD3/NAND_WP/HPS_GPIO27	Bank7B
265	A13	I/O	RGMII1_MDC/NAND_DQ2/I^2C3_SCL/HPS_GPIO21	Bank7B
267	E16	I/O	RGMII1_MDIO/NAND_DQ1/I^2C3_SDA/HPS_GPIO20	Bank7B
269	A12	I/O	RGMII1_TX_CTL/NAND_DQ4/HPS_GPIO23	Bank7B
271	J15	I/O	RGMII1_TX_CLK/NAND_ALE/HPS_GPIO14	Bank7B
273		PWR_{OUT}	VIO_7B7D_+1.8V[25]	Power
275	D17	I/O	RGMII1_TXD3/NAND_RB/HPS_GPIO18	Bank7B
277	A15	I/O	RGMII1_TXD2/NAND_RE/HPS_GPIO17	Bank7B
279	J14	I/O	RGMII1_TXD1/NAND_CLE/HPS_GPIO16	Bank7B
281	A16	I/O	RGMII1_TXD0/NAND_CE/HPS_GPIO15	Bank7B

[24] BOOTSEL1 is used locally on the SOM for the QSPI_SS0 select line. It is available to the edge connector after a 10KΩ series resistor. Pull this pin high to VIO_7B7D_+1.8V or low to GND to define BSEL1.

[25] The voltage rail for HPS Bank7B and Bank7D is generated by the SOM. The standard products use a +1.8V I/O rail for these banks to conserve power. If using Bank7B connections, the I/O voltage for the RGMII Phy or NAND device can be driven by the power supply output from the module.

+2.5V Exposed to use as a +VIO Enable

BANK 4A IO Voltage
+1.2 - 3.3V/300mA
Powers VCCPD3B4A when >2.5V
VCCPD3B4A adds up to 145mA

BANK 3B IO Voltage
+1.2 - 3.3V/250mA
VCCPD3B4A from +VIO_4A if >2.5V

BANK 8A IO Voltage
+1.2 - 3.3V/50mA
Powers VCCPD8A when >2.5V

B4A_RZQ0 is on B41_N - connect to precision resistor for OCT ref
if RZQ OCT used, tie B41_P to GND to avoid aggressor signal

THESE ARE BYPASSED WITH A SMALL CAP FOR A
RETURN CURRENT PATH FOR ADJACENT SIGNALS

CLK2p is used for
FPGA DDR RefClk

B3A are Not Connected in
modules with FPGA DDR

BANK [3A|5A|5B] IO Voltage
+1.2 - 3.3V/150mA
Powers VCCPD[3A|5A|5B] when >2.5V

Additional GXB channels
possible in larger future module.

E1/E2 Reserved for future high power modules
MXM v3.1 Specifies 7.20V at up to 10A

5.0V +/-6%
2.5A

LEGEND

- FPGA CONFIG MODE SELECT - DIRECT TO POWER/GND
- Available on Expanded I/O Modules w/o FPGA DDR Memory
- POSSIBLE FUTURE MODULE VARIANTS
- THESE PINS ARE NEVER EXPOSED

Title: *MitySOM-5CSx - Ext Interface*			Critical Link, LLC 6712 Brooklawn Parkway Syracuse, NY 13211 315.425.4045 www.criticallink.com
Size: C	Number: 80-000772RI-2	Revision: C	
Date: 3/19/2015	Time: 12:08:00 PM	Sheet 2 of 9	
SVN: 2349	File: cvsx_ext_interface.SchDoc		

2.2 Module Reset

Both reset connections are available on the edge connector. The Power-On-Reset, or Cold reset is asserted active-low at power-on until all the monitored power supply rails are alive. Note that this include the V_{CCBAT} connection and the device will not come out of reset without this supply powered up.

The Warm reset is also available as a less severe reset signal. Consult the Altera documentation for the differences between the two reset signals. Note that both resets are active-low and can be read or driven by the MitySOM. These should be driven by an open-collector output and pull-up resistors are included on the module, so they are not necessary on the carrier board.

2.3 JTAG / TRACE

The JTAG connections are routed to a debug header on the MitySOM-5CSx. These can be accessed through a simple JTAG breakout board available in the MitySOM-5CSx Dev Kits or using a MitySOM-5CSx JTAG/TRACE high speed debug adapter. The TRACE interface can be routed to the debug header on the SOM instead of the edge connector for a high-bandwidth trace interface. This requires additional ARM debug hardware to take advantage of, but the debug adapter also includes the BlasterII interface for high speed debug.

2.4 Module Boot Configuration

Boot options are defined by three sets of inputs: MSEL, BSEL, and CSEL. MSEL defines the FPGA configuration scheme. BSEL identifies the boot device to try first for the HPS. Note that the HPS will try additional boot sources if the boot selection initially fails. CSEL is the clock selection and defined the clock divisors to use after reset.

Defining the desired FPGA configuration mode is is done through the MSEL input pins. These are dedicated inputs that need to be connected to power or ground with low impedance paths. Additionally, they need to be valid at power-on and the high state cannot be gated by the I/O power enable.

The BSEL inputs are multi-function pins. At reset, they are read to determine the desired boot device. After reset, they are used for other I/O functions. These should be pulled high or low through 1KΩ or higher resistors. The BSEL nets are in the power domains of their respective Banks in the FPGA. BSEL0 is in Bank7A and powered by +3.3V (VIH > 2.1V). The other two, BSEL1 and BSEL2 are in Bank7B powered by 1.8V. The 1.8V is provided by the SOM for IO power, such as used on the RGMII Ethernet interface. If you want to pull these to +3.3V, that is OK as long as you limit the current to below 8 or 10 mA worst case. Pull-up / pull-down values of 1KΩ and 10KΩ are very safe. BSEL1 has a 10KΩ series resistor making it safe to tie directly high or low – even if high is +3.3V. This signal is used for QSPI_SS0 after reset on the SOM itself and the 10KΩ makes sure there is isolation for running the QSPI interface. The series resistor does not impact the pull-up/pull-down as minimal current is pulled, so the same resistor scheme can be used.

Lastly, the CSEL inputs define the clock scheme coming out of reset. These are also multi-function pins, read during reset and other Bank7A I/O pins after reset. Being in Bank7A, their power domain is +3.3V. Add a pull-up or pull-down resistor to define the desired clock option.

Altera has identified an errata with the HPS PLL where it will sometimes fail to lock at reset. When this happens the HPS may hang during the BootROM stage and fail to proceed to the Preloader, or it may fail SDRAM calibration during the Preloader. To avoid this errata, follow the workaround provided

by Altera[26]. This includes setting the CSEL to 00 to bypass the PLL at reset and apply the patch to the Preloader.

See Altera's Booting and Configuration guide for more information[27].

3 Electrical Requirements

3.1 Power Supplies

The module takes 5V power in and generates all the supply rails required for the FPGA core and HPS peripherals. The I/O Voltages have been exposed to the edge connector to support the wide range of I/O standards that are available.

3.2 Power Sequencing

The Cyclone V supports any power sequence, but there is some benefit in sequencing the module power followed by the VIO power supplies. To support this sequencing, there is a VIO-ENABLE signal on the edge connector that indicates when the core voltages and aux supplies are up. Once this signal is high, the VIO supplies should be enabled to complete the power-up sequence.

3.3 I/O Interfaces

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{IN}	Module Input Voltage	4.85	5.0	5.15	V
I_{IN}	Module Input Current	—	—	2.5	A
	5CSX-H6-42A	—	—	~2	A
	5CSE-L2-3XA	—	—	~1	A
	5CSX-H6-53B	—	—	~2	A
V_{CCPD}	I/O pre-driver (VIO > 2.5V)	2.85	3.0 or 3.3	VIO	V
	I/O pre-driver (VIO $\leq$ 2.5V)	—	2.5	—	
V_{CCIO}	I/O buffers (1.2-3.3V)	1.14	1.2 to 3.3	3.465	V
V_{CCBAT}	Battery back-up power supply (For design security key and RTC)	1.2[28]	—	3.0	V
V_I	I/O Pin DC Input Voltage	-0.5	—	3.6	V
V_O	Output Voltage	0	—	VIO	V
T_J	Operating Junction Temperature				
	(CT)	0	—	85	°C
	(IT)	-40	—	100	°C
	(AT)	-40	—	125	°C
t_{RAMP}	Power Supply Ramp Time	0.2	—	4	ms

[26] http://www.altera.com/support/kdb/solutions/rd06202014_496.html
[27] http://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/cyclone-v/cv_5400A.pdf
[28] At V_{CCBAT} of 1.2V to 1.5V, the minimum JTAG TCK clock period is extended to 167 ns. See *cv_51002* for details.

3.4 I/O Protection

- Limit Bank connections to the Bank's I/O Voltage.
- Connect a 1KΩ series resistor to +5V_USB_VBUS to avoid the danger of any possible connection to the adjacent GND. The module only needs to sample the voltage for controlling the USB phy.

3.5 Battery Backup

There is a very low power RTC on the MitySOM module. The +3VBAT input provides the battery backup power for the RTC along with the VBAT connection on the Cyclone V. If a battery is not used, connect this line to +2.5V or +3V. The recommended electrical range for the battery has a maximum of +3.0V, but the absolute max spec is 3.9V.

4 Mechanical Requirements

4.1 Module Connectors

The MitySOM-5CSx uses the physical MXM 3.0 standard edge connector for the module I/Os. The recommended initial connector is *MM70-314-310B1-1-R300* from JAE Electronics. Other standard MXM 3.0 connectors are expected to be compatible. If using another connector, ensure the pins at the opposite end of the main ganged power input (pins E1, E2, E3 and E4) are individual pins. According to the MXM specification, the top edge connector row has the two end pins tied together. However, on the MitySOM, these are two separate pins. If they are ganged and the recommended series resistor is included, the USB1 interface will not power up, but otherwise should cause no damage.

4.2 Mounting Methods

The MXM connector has no latch arms for retaining the module. Instead, there are two corner mounting holes for securing the module. This provides a secure means of fastening the module in an embedded design for reliable performance.

4.3 Shock & Vibration

This section will be filled in with additional shock and vibration test data.

5 General Design Guidelines

http://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/cyclone-v/cv_51001.pdf "Cyclone V Device Overview"

Table 25: FPGA Bank Pin Allocations

	Bank Package U23 Fabric Size	FPGA DDR U672 85/110kLE	Exp I/O U672 25/40kLe	Exp I/O U672 85/110kLe
FPGA I/O Bank	3A-FPGA DDR	15	–	–
	3A-Edge Pins	1	16	16
	3B	32	32	32
	4A	68	68	68
	5A-FPGA DDR	16	–	–
	5A-Edge Pins	–	16	16
	5B-FPGA DDR	7	GND	–
	5B-Edge Pins	–	GND	–
HPS Row I/O Bank	6A	56	56	56
	6B	44	44	44
HPS Column I/O Bank	7A	19	19	19
	7B	22	22	22
	7C	12	12	12
	7D	14	14	14
FPGA I/O Bank	8A	6	6	6
	8A-Grounded IOs	N/A	7⇒GND	N/A
	Total	312	305	305

5.1 Pin Allocation

5.1.1 HPS Peripherals

- TRACE MUX

5.2 FPGA Size Migration Guide

The family of MitySOM-5CSx modules was designed to be pin compatible. As a design migrates between different modules within the MitySOM-5CSx family, there are some interfaces that are no longer available. There are also a few pins that become ground pins due to the U672 FPGA package pin migration limitations.

5.2.1 High Speed Transceivers (GXB)

The first major option is whether or not the high speed transceivers (GXB) are included on the module. The models that include the GXB interfaces have model numbers starting with 5CSX, and the 5CSE models do not include the GXB interfaces.

Altera recommends connecting the GXB interface inputs to GND through 10kΩ resistors. This keeps the inputs safe, quiet and can save some power as well.

5.2.2 FPGA DDR or Expanded I/O

The next feature selects either FPGA DDR or Expanded I/O edge connections. The FPGA DDR is a DDR3 memory connected to Banks 3A/5A/5B FPGA fabric I/O pins. The Bank 5B I/O pins are not available on the smaller 25kLE and 40kLE FPGA size devices, so FPGA DDR is only supported on the large device models with 85kLE or 110kLE FPGAs.

When the FPGA DDR memory feature is removed, it can be replaced by Expanded I/O connections to the edge connector. The Expanded I/O feature makes an additional 26 pins available from Banks 3A and 5A. See Section subsection 6.8 for details on the additional edge connections available with Expanded I/O. The additional pins also make it possible to use some of the advanced configuration options with the module, such as partial reconfiguration and the wide x16 configuration interface.

With the Expanded I/O feature, there is an additional VIO power connection to define the I/O voltage used by the additional FPGA Bank 3A and 5A pins. Make sure the power is supplied on the additional VIO_3A5A5B edge connector pin. The modules without the Expanded I/Os have no connection to this pin to provide safe migration across the MitySOM-5CSx family modules.

5.2.3 Bank5B and Bank8A Pins

If planning to migrate between small and large FPGA size options, beware of the 7 Bank5B pins that become ground on the 25kLE and 40kLE FPGA sizes. These pins are only used by the FPGA DDR memory option, as available on some large FPGA, 85kLE or 110kLE, modules. The Expanded I/O connections avoid these pins. Also note that on small FPGA, 25kLE and 40kLE, modules there are 7 Bank8A pins that are I/O pins instead of the ground pins they are on the large FPGA package. These pins must not be used as outputs; they are connected directly to ground on the MitySOM module. See Table 26 for the pin details.

Table 26: Expanded I/O Ground Pins

U23 BGA Pin	Bank	25kLE/40kLE	85kLE/110kLE
W20	5B	GND	I/O (FPGA DDR/No Connect)
W21	5B	GND	I/O (FPGA DDR/No Connect)
W24	5B	GND	I/O (FPGA DDR/No Connect)
Y24	5B	GND	I/O (FPGA DDR/No Connect)
AA26	5B	GND	I/O (FPGA DDR/No Connect)
AB26	5B	GND	I/O (FPGA DDR/No Connect)
AB25	5B	GND	I/O (FPGA DDR/No Connect)
L9	8A	GND (I/O)	GND
L10	8A	GND (I/O)	GND
H5	8A	GND (I/O)	GND
H6	8A	GND (I/O)	GND
K8	8A	GND (I/O)	GND
L8	8A	GND (I/O)	GND
H4	8A	GND (I/O)	GND

5.3 Power and Heat Dissipation

6 Schematic Guidelines

6.1 Reset

The reset lines include pull-up resistors on the module tied to +3.3V. This is the last supply to start and will keep the reset active until all the power supplies are started. If additional pull-up resistors are added to the

6.1.1 Power-On Reset (POR)

The power-on reset is an input-only signal with a pull-up resistor to +3.3V on the module. This input can be driven low to force a cold reset, placing the SoC in a mode equivalent to the power-on state. This should be driven with an open collector signal if actively driven.

6.1.2 Warm Reset (RST)

The warm reset is a bidirectional signal. A reset monitor is recommended, but not required. When choosing the reset monitor, choose one with an open collector output to avoid contention on the line. This input can be driven low, but avoid driving it high – the pull-up on the module will provide the high level once the power supplies have all started up.

6.2 Power Input

The main power source for the MitySOM is the +5V input. There are additional voltage connections on the edge connector to power the FPGA I/O banks to allow the full range of voltage standards supported by the Cyclone V FPGAs.

Review the Cyclone V power guidelines for supporting multiple voltage standards. . .

6.3 Power Sequencing

The Cyclone V is designed to allow any sequence when applying power. With that said, it is generally advised to power the core voltages before the I/O voltages. There is a +2.5V_ENABLE output from the module to help sequence the power supplies. On the module, the core voltage comes up followed by the +2.5V and DDR memory supply rails. Delaying the external I/O voltages until the +2.5V_ENABLE signal is active will save some extra power draw at start-up.

6.4 Bank 7B and 7D Power

The HPS banks that connect to the QSPI NOR Flash and USB on the MitySOM module are powered by +1.8V to save some power. The RGMII interface to a Gb Ethernet Phy shares Bank 7B with the QSPI NOR flash interface, and therefore the +1.8V bank voltage is used. To avoid requiring an additional power supply on the baseboard, there is a +1.8V output provided to power a Gb Phy.

If there are more devices running from +1.8V on the baseboard, a separate power supply is advised. The baseboard is expected to be able to dissipate the heat of additional loads better than the module due to size constraints.

6.5 MitySOM-5CSx VIO Support

The module includes power inputs for the I/O banks to support the wide range of voltage standards available in the Cyclone V FPGAs. The carrier board simply needs to identify the I/O standards required by a design and supply the voltage required. The banks have separate rails and Bank4A can use a different VIO voltage than Bank3B. Note however, that these two banks share a predriver rail, so if +3.0V or +3.3V is desired, both banks must use the same voltage. If the VIO voltage is +2.5V or lower, the banks can be powered separately.

The Cyclone V FPGA requires a predriver voltage to support the I/O voltage for each bank. To simplify this and conserve the precious edge connector pins, the VCCPD rail is handled on the module and meets the requirement of the VIO rail supplied across the full range of support from the minimum to the +3.3V max VIO voltage. Simply make sure that the VIO supply can supply the additional current of the VCCPD rail if the VIO voltage is above +2.5V.

One common standard that will be used in many designs is LVDS. The Cyclone V supports on chip termination for the LVDS pairs, which simplifies the required board design. If this is desired, make sure the VIO voltage is +2.5V, or the on chip terminations cannot be used.

6.5.1 VCCPD Power and Support for +3.0 or +3.3V Standards

The I/O banks were designed with +3.3V support in mind. The VCCPD rails are driven by the internal +2.5V regulator until the IO bank voltage goes above it, then it switches to the supplied +VIO input for the bank. Since banks 3B and 4A share VCCPD, the Altera rules must be followed: if +VIO_3B or +VIO_4A are higher than 2.5V, they both must match (3.0V or 3.3V). In this case, the VCCPD3B4A is supplied by +VIO_4A when above +2.5V for the I/O voltage. It is expected that the +VIO_3B and +VIO_4A will be driven by the same supply when using these higher voltage standards. Avoid driving these two banks from separate supplies when the +VIO_3B or +VIO4A voltage is above +2.5V.

The lower voltage standards are supported as well by the built-in +2.5V minimum on the VCCPD rail. The I/O standards at 2.5V and below can be mixed among the banks following Altera's rules.

The VCCPD8A uses another instance of that power switching to run that bank's voltage separately with the desired voltage standard specific to your application. Again, this will switch the VCCPD8A between a minimum of the +2.5V supply or a higher +VIO_8A voltage to support the standards above +2.5V.

6.5.2 +2.5V VIO on the Development Board

The Dev Board uses +2.5V for the I/O banks:

- VIO_4A
- VIO_3B
- VIO_8A
- TP4

It also uses this rail for a couple pull-ups on the PCIe interface. These will not cause an issue as they are weak pull-ups and mostly connected to bank 4A. The PERSTn signal does go to Bank5A on a lower voltage, but will be safe because it is a small enough current. The one area where there is a limitation concerns the X101 clock input. This is an LVDS clock source and may not be usable with higher I/O voltage levels, but the boards will not be damaged.

If a different voltage standard is desired on the FPGA IOs, the voltage feedback can be adjusted on the switching supply U601 (R603, R613, and R616). Adjusting this will change the voltage on all three banks routed to the edge connector and will impact the I/O signals on both HSMC connectors. The FPGA design will need to specify the appropriate I/O standards on all three banks as well.

6.5.3 VREF Connection and Mixed I/O Standards

The VREF connections are tied to voltage dividers that supply a reference voltage set to half the VIO voltage for each bank. This covers the most I/O standards without consuming the limited edge connector pin resources. This does however, impede the use of mixed standards for supporting lower voltage input standards on a higher voltage bank. If an application requires this feature, please contact Critical Link for further support.

6.5.4 Testing

The development board has been tested with the full range of I/O voltage standards to verify the VCCPD switching to validate the design. There are no known issues with supporting the full range of I/O voltage standards.

6.5.5 Follow Altera Guidelines for 3.0V and 3.3V I/O Standards

Refer to Altera's documentation for additional details:

I/O Features in Cyclone V Devices (*CV_52005*)
http://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/cyclone-v/cv_52005.pdf

- Table 5-10: MultiVolt I/O Support in Cyclone V Devices
- Page 5-11: I/O Design Guidelines for Cyclone V Devices
- Page 5-18: Guideline: Observe Device Absolute Maximum Rating for 3.3 V Interfacing
- etc.

  Guideline: Observe Device Absolute Maximum Rating for 3.3 V Interfacing

  To ensure device reliability and proper operation when you use the device for 3.3 V I/O interfacing, do not violate the absolute maximum ratings of the device. For more information about absolute maximum rating and maximum allowed overshoot during transitions, refer to the device datasheet. Perform IBIS or SPICE simulations to make sure the overshoot and undershoot voltages are within the specifications.

6.6 VBAT Battery back-up power supply

The VBAT powers the RTC on the MitySOM as well as the VBAT connection on the Cyclone V used for security features. When a design does not require the design security feature or real time clock,

connect VCCBAT to a 1.5-V, 2.5-V, or 3.0-V power supply. The power-on reset (POR) circuitry monitors VCCBAT. Note, the Cyclone V devices do not exit POR if VCCBAT is not powered up.

6.7 Configuration Options

6.7.1 PROM

The FPGA can be configured from a configuration prom by connecting up the configuration interface exposed on the bottom edge connector pins 27 through 43.

6.7.2 Partial Reconfiguration

Externally supported on Expanded I/O versions of the module. This requires MSEL set to the FPP x16 mode. See Altera's Cyclone V manual: cv_5v1.pdf[29] along with the Booting and Configuration section of the Handbook[30].

6.8 Expanded I/O Connections

There are versions of the MitySOM-5CSx module that expose more I/O pins. This is accomplished by removing the single chip FPGA DDR interface and exposing the pins to the edge connector instead of using them for the internal FPGA DDR memory. For a list of the additional connections made available, see Table 27.

With this change, an additional VIO voltage input is exposed. This allows the new banks' pins to run on a separate I/O standard than the other banks if desired.

These additional pins also expose the additional configuration options. If an application needs to be configured as fast as possible, or manage partial reconfiguration through the configuration pins, this is supported in the models with expanded I/O instead of the dedicated FPGA DDR memory.

6.9 PCIe Hard IP

The PCIe Hard IP can be configured to run a x1, x2, or x4 PCIe interface. It will generally be a root port, but can also be configured as a peripheral endpoint device. When used as an endpoint, the configuration via protocol (CvP) is supported by the production silicon modules.

If planning to use the Hard PCI Express controller, use the low transceivers and reference clock. The PCI Express reset signal is on Bank5A and is available on the edge connector for modules that have less than 512Mb of FPGA DDR. When the FPGA DDR memory is 512Mb or larger, that additional pin is required for addressing the DDR memory. This PERST# signal is within the +1.35V VIO of Bank5A for the modules with FPGA DDR. In the future modules, with the FPGA DDR memory interface replaced with additional I/O pins, this signal will be on the +VIO–3A5A5B voltage rail provided by the carrier board. Configure this pin as an open collector and drive it low when active or let it float high with the external pull–up resistor. The voltage on this I/O is safe with a 10KΩ pull-up resistor – even to +3.3V.

[29] https://www.altera.com/en_US/pdfs/literature/hb/cyclone-v/cv_5v1.pdf
[30] https://www.altera.com/en_US/pdfs/literature/hb/cyclone-v/cv_5400A.pdf

Table 27: Expanded I/O Pins and Wide Configuration Connections

Edge Pin	Bank	Expanded I/O Signal	Config
47	5A	B5A-TX-R1-P	
49	5A	B5A-TX-R1-N	PR–REQUEST
53	5A	B5A-TX-R3-P	nCEO
55	5A	B5A-TX-R3-N	CvP–CONFDONE
42	5A	B5A-TX-R5-P	DEV–OE
44	5A	B5A-TX-R5-N	DEV–CLR#
181	3A/5A/5B	+VIO-3A5A5B	
183	5A	B5A-RX-R2-P	INIT–DONE
185	5A	B5A-RX-R2-N	CRC–ERROR
187	5A	B5A-RX-R4-P	
189	5A	B5A-RX-R4-N	
191	3A	B3A-RX-B7-P	PR–ERROR
193	3A	B3A-RX-B7-N	PR–DONE
195	3A	B3A-RX-B5-P	CLKUSR
197	3A	B3A-RX-B5-N	DATA14
199	3A	B3A-RX-B3-P	DATA12
201	3A	B3A-RX-B3-N	DATA10
203	3A	B3A-RX-B1-P	DATA8
205	3A	B3A-RX-B1-N	DATA6
182		GND	
184	3A	B3A-TX-B8-P	
186	3A	B3A-TX-B8-N	PR–READY
188	3A	B3A-TX-B6-P	DATA15
190	3A	B5A-TX-B6-N	DATA13
192	3A	B3A-TX-B4-P	DATA11
194	3A	B3A-TX-B4-N	DATA9
196	3A	B3A-TX-B2-P	DATA7
198	3A	B3A-TX-B2-N	DATA5

6.10 Assigning I/O Pins

Besides the HPS peripherals, there are multiple banks available for the I/O pin assignments. To identify the best pin assignment option, try to follow the guidelines below. The simplest path is if all the I/Os use the same VIO voltage, so that is addressed first. For

6.10.1 All FPGA Fabric I/O Pins on a Single VIO Voltage

An example of this case would be a mix of +2.5V LVCMOS or LVTTL signals along with LVDS differential pairs. If using LVDS pairs, read the notes in the LVDS section under Layout Guidelines.

Start with the highest bandwidth signals. Identify the clocking scheme that will be used for these high bandwidth interfaces. Note that the clocks are distributed efficiently in quadrants within the FPGA. If the clock needs to cross the quadrant boundary, it goes through a clock crossing and there will be additional jitter and more difficulty in meeting timing in the FPGA design. The best performance

is achieved when the clock is brought in on a dedicated clock input pin or pair of pins. It is highly recommended that the data pins associated with that clock are in the same quadrant. When assigning clock pins, note that there is only one dedicated clock route to the fractional PLL for each clock input pair. If using a single-ended clock input, choose the positive input pin of the clock pair because this has the connection to the dedicated clock route. The negative input of the pair will use an more general clock routing resource to reach the fPLL and incur additional jitter.

If additional clock inputs are required, they can be used directly on other input pins, but cannot be routed to fPLLs. Non-dedicated input pins and logic can drive regional clock resources.

Once the clock is identified, assign the data pins. For any inputs that need the extra bandwidth available by using the SERDES blocks, make sure they are assigned to pin locations that include the proper dedicated SERDES signaling direction. Once the first interface is allocated, build up a simple FPGA project and verify the pin allocation and timing constraints can be met.

Use the Quartus TimeQuest Timing Analyzer Wizard to generate the clock constraints for the design. Use the Quartus Pin Planner to assign the pins allocated in the design. For the data lanes, connect up some simple logic that instantiates the SERDES blocks as necessary for the design and consumes the data or generates data for an active design. Once the prototype logic is ready, compile the design and make sure the pin assignments are valid and the logic did not get stripped out due to constant values or lack of a data consumer.

Once the first interface is prototyped and pin assignments are validated, move on to the next interface. Work through each group of signals ans adjust the assignments as necessary to meet the rules and timing requirements for the design.

6.10.2 Multiple I/O Voltage Standards

The MitySOM was designed to support the various I/O voltage standards that are supported by the Cyclone V FPGA. Refer to Altera's documentation for details of supporting multiple standards within a bank. The initial MitySOM-5CSX offering has three separate I/O bank voltages. The main issue to be aware of when using different bank voltages is that Bank3B and Bank4A share a predriver voltage. At 2.5V or lower, Banks 3B and 4A can use separate I/O voltage rails. At voltages higher than 2.5V, Banks 3B and 4A must be set to the same I/O voltage.

6.10.3 Accessing More of the HPS Peripherals

The HPS pin MUX options have limited means of connecting directly to the hard MAC blocks in the HPS. For example, a typical design will use one RGMII Ethernet interface and the module's included USB interface. With these two interfaces assigned, there is no place to bring out the second of either directly on the HPS pins.

These additional peripherals can still be utilized and the design can take advantage of the Hard MAC blocks. The FPGA design can pass the additional peripheral connections to the FPGA fabric and use the FPGA I/O pins to connect to the Phy.

6.10.4 Additional FPGA I/O Pins

A similar need may be a design that requires additional FPGA I/O connections instead of the HPS Peripherals. The HPS pins that are connected to the edge connector can be passed to the FPGA fabric instead of controlled by the HPS peripherals. To use this feature, the Loan-IO settings would be used in

the HPS settings under QSYS. Note that these pins may be more difficult to work with for higher speed interfaces. It is recommended to build the FPGA design in Quartus to validate the timing constraints before committing to the PCB.

7 Board Layout Guidelines

7.1 Power Supply and Decoupling Capacitors

Switching supplies are recommended as the best design practice. These reduce wasted power and result in a better product design. As temperature increases in a design, the cooling requirements become more onerous. Higher temperatures also increase part failures and reduce the MTBF of a design. When designing the layout of a switcher power supply, pay particular attention to the high current switching loops through the supply, inductor, and caps at the output. The input has similar current loops to supply the power and there needs to be small, fast response, caps close to the power supply input pins and the larger bulk capacitor can be placed a little farther away. Keeping these current loops small will result in a more stable design that also minimizes EMI challenges.

Ensure the power supplies have sufficient capacitance. The design must include a good mix of high frequency ceramic caps close to the power pins as well as the slower large bulk caps to maintain the rails. For best results, place vias to the side of capacitor footprints instead of at the ends. Also, keep the power and ground connection vias close to the capacitor footprint. Use wide and short traces for power supplies and return paths.

7.2 Critical Routing

As interface speeds increase, the board layout becomes increasingly important. To have a successful design, ensure there is a solid reference plane under all high speed signals. These include any signals running at speeds of 100MHz or higher when short traces can be used. This requirement extends to slower signals as the trace length increases. For best results, keep the wide bus interface and high speed signals short.

7.2.1 Controlled Impedance

Particular attention should be payed to high speed interfaces concerning trace geometries as well. In general, design the trace size and board stack-up with a target impedance of 50Ω for single ended signals or 100Ω for differential pairs. If there are bus interfaces with a common clock for a set of data lanes, route them with matched length traces as necessary.

For the high-speed transceiver signals, have the PCB fabricated using controlled impedance. Most of the high speed transceiver configurations do not require tight matched length traces, but they should not differ in length significantly.

7.2.2 RGMII Ethernet Interface

When using an RGMII Ethernet interface in the design, pay particular attention to the routing of the RGMII signals. These need a continuous reference plane under the traces and a couple GND vias at the layer transitions. Make sure there is a reasonable path from the edge connector GND to the GND

reference plane near the RGMII nets. Length matching is important for these signals as well. The differential pair lengths from the Ethernet Phy should be extended instead of the wide single-ended RGMII bus if the Ethernet jack is too far away from the SOM. The RGMII signals are around 3 inches in length on the MitySOM. For best results, keep the RGMII traces less than 2 inches in length.

Also important when routing the RGMII Ethernet signals is to avoid crosstalk. Route the traces with a target impedance of 50Ω. Keep the routes short and match the length – the transmit group of signals and the receive group can have different lengths as long as the group has matched length. To avoid crosstalk, try for trace separation of 3 times W, the trace width. If space constrained, try to maintain at least 2W separation on parallel traces.

When the layout is fully routed, review the Ethernet signal groups and make sure the crosstalk is minimized. Also verify there is a continuous reference plane under the path of the RGMII signals.

7.2.3 Debugging a Bad RGMII Layout

Sometimes a bad layout has already been released and needs to be recovered if at all possible. If the Ethernet works at 100Mb/s, but not very reliable at 1Gb/s, try adding RC termination to the RGMII nets on the baseboard. If reading this design guide after the problem is in-hand, try the following suggestions to see if the design can limp along until the next board spin.

The current suggestions for terminating the RGMII nets is to use RC termination at the end of the RGMII route near the Phy with values of 75Ω to 10pf to GND in series at the end of the route for RC parallel termination. When trying to recover the design, start with terminating the signals next to the CLK lines and the CTL lines. The clock needs to be clean and adding the RC termination to it will probably slow it down too much and make the interface worse. The CTL lines (RX_CTL and TX_CTL) include the error flag an data valid signals. If this signal gets registered wrong, the packet gets tossed. If this does not work, next try adding RC termination to the other data lanes and give it a try.

7.3 LVDS Interfaces for High Bandwidth

The Cyclone V include SERDES blocks for high speed serialization and deserialization. These hard IP blocks are included in most of the fabric I/Os. Note however, that each pair can only operate at the highest data rates in one direction. All the LVDS pairs can be input or output, but there is additional bandwidth available if the SERDES block is utilized in the design.

To ease design of boards that require the highest bandwidth, the LVDS pairs have been noted on the edge connector to include the higher performance SERDES direction. In general, the SERDES TX pairs are on the top edge connector pins and the SERDES RX pairs are on the bottom edge connector. There are a couple exceptions to this. The Bank8A clock pairs are in a very limited bank and do not fully follow the TX/RX edge assignments. There are two extra TX pairs available on the 5CSx expanded I/O modules that also break this pattern. The remaining fabric I/O pins do follow the intended pattern. This includes all the signals on Bank3B and Bank4A as well as the expanded Bank3A signals and the remainder of Bank5A signals. One other point to note is that not all of the Bank4A TX signals have pairs. All the Bank4A I/O pins are exposed, but on the Cyclone V package used on the MitySOM-5CSx modules, there are 6 pins that are not paired up.

The Cyclone V FPGA has some pin allocation requirements that define how a mix of single ended I/O pins and differential pairs can be placed. Before releasing a board design for fabrication, prototype the FPGA design enough to validate the pin assignments. Verify all the pin assignments are defined in a Quartus project and make sure a successful build can be generated. Also, pay particular attention to

the clocking scheme and prototype the design with the desired clocking scheme. For additional details on the I/O restrictions and pin placement guidelines see the Cyclone5 Handbook[31].

7.4 Return Currents

The module's edge connector has GND connections distributed along the interface pinout to maintain signal integrity. These connections should be connected to a solid ground plane to create an efficient return current path. For some additional return current paths to help with the switching edges, 1000pF caps have been included on specific nets. These are on the module and should be added to the I/O board as well similar to the Dev Board. The return current caps are helpful on the following signals:

- RTC_PSW
- USB_FAULTn
- MSEL[0-4]
- BOOTSEL1

When placing these capacitorss, keep them close to the edge connector as much as possible. Also, place the via for each capacitor to the side of the pads with short traces to a via to a power or ground plane. This minimizes the inductance parasitics and improves the AC return current path.

Two of these signals are next to the last high speed transceiver pair. If that transceiver is used in the end application, particular attention should be paid to the return current capacitor on the `BOOTSEL1` and `USB1_FAULTn` connections. The next important one is the `RTC_PSW` capacitor connection if an SDMMC interface is used in the design. This sits next to the SDMMC_CLK running at up to 108MHz. The other return current caps are less critical.

8 Thermal Management

The thermal management of the full system should be considered carefully to create a reliable end product. With the MitySOM-5CSx module in a system, the FPGA is likely a large part of the control unit for a product. It has a wide range of power consumption that is defined by a number of factors specific to each application.

Users need to review the power consumption for their target application and address the thermal management as well. Some references are available to help identify the amount of power and heat generated by the FPGA. On the module, the power supplies and interfaces were designed with efficiency in mind. The power supplies typically operate better than 90 percent efficient and the voltage rails have been chosen to limit the power required for the included interfaces. The one exception is the +3.3V linear supply, but this only powers very light loads.

AN 358: Thermal Management for FPGAs (PDF) http://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/an/an358.pdf

AN 185: Thermal Management Using Heat Sinks - Altera http://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/an/archives/an185.pdf

High-Speed Board Design Advisor: Thermal Management http://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/tb/tb-093.pdf

[31] http://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/cyclone-v/cyclone5_handbook.pdf Cyclone V Handbook, CV-52005, 2014-06-30, Section 5-20 Guidelines.

8.1 Package and Thermal Resistance

The following table has information obtained from Altera's website through the following URL. It includes the thermal resistance as measured according to the JEDEC JESD51 standard. These numbers were obtained using the 2s2p board specification. This is a 4-layer board with the two signal layers on the outside and the two plane layers on the inside. The MitySOM is smaller than the JESD51-9 Area Array SMT Test Board size of 101.5mm x 114.5mm and the additional components on the module such as the DDR memory and power supplies also contribute to the thermal performance. The one improvement over the 2s2p test board is the solid copper plane on the top and bottom layers. This will help spread the heat and efficiently transfer it to the air as much as possible. The Table 28 provides an idea of thermal performance under a few different test conditions, but the specific testing of the end product is the user's responsibility.

http://www.altera.com/support/devices/packaging/specifications/pkg-pin/dev-package-listing.jsp?device=Cyclone_V

Table 28: MitySOM-5CSx FPGA JEDEC JESD51 2s2p Thermal Resistance

Device	Package-Pins	Condition	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)
5CSEBA2	UBGA-672			7.5	3.4
		Still Air	18.1		
		100 ft./min	16.2		
		200 ft./min	14.3		
		400 ft./min	12.8		
5CSXFC6	UBGA-672			6.1	2.6
		Still Air	16.0		
		100 ft./min	14.8		
		200 ft./min	13.0		
		400 ft./min	11.5		

Additional information is available through Altera's website:

Power Management Resource Center
http://www.altera.com/support/devices/power/pow-power.html

8.2 Module Thermal Information

The information in Table 30 and Table 31 is provided to give an idea of a maximum power consumption for a demanding application. For best results, the Early Power Estimator should be used with details for the specific application. The numbers in Table 30 include all the interfaces on the module as well as an RGMII interface to represent a reasonable maximum, but the Phy would reside on the carrier board. The Bank3B and Bank4A I/O interfaces are dependent on the carrier board design and are not included in the calculations. This is limited to I/O power for those banks and that power will minimally contribute to the heat load of the module. The one exception that should be noted is the power consumed in the on chip termination if used in a design.

The EPE spreadsheet provides various application benchmarks for checking HPS power consumption. The information should be filled out and calculated for the specific application needs as there is a wide range of power the device could consume. For some ways to save power, it is possible to run the HPS and logic at lower clock rates to save power.

[32]The minimum power for the 5CSE-S2-3XA is expected to be around 1.2W to 1.5W with the HPS running at 300MHz, with

Table 29: MitySOM-5CSx Nominal Power

SOM	State	Typ (W)	MHz	Board
5CSX-H6-42A	Reset	0.95	800	SOM Only
	Linux Idle	2.58	800	SOM Only
	uBoot Unconfigured	2.94	800	SOM Only
5CSX-H6-53B	Linux Idle		800	SOM Only

Table 30: MitySOM-5CSX Power Ranges

SOM	Subsystem	Minimum [32]	Maximum	UNIT
5CSX-H6-42A	Static HPS	0.025	0.05	W
	HPS		1.06	W
	Static FPGA Fabric	0.539	0.78	W
	FPGA		3.65	W
	GXB		0.46	W
	PCS and HIP		0.29	W
	DDR–Background	0.335	0.34	W
	DDR–Activate	0.181	0.91	W
	DDR–RD/WR/Term	0.127	1.01	W
	Power Supplies		TBD	W
	Other		TBD	W
	———————-	———	———	
	Total		**8.55+**	W
5CSX-H6-53B	Static HPS	0.025	0.05	W
	HPS		1.06	W
	Static FPGA Fabric	0.539	0.78	W
	FPGA		3.65	W
	GXB		0.46	W
	PCS and HIP		0.29	W
	DDR–Background	0.466	0.47	W
	DDR–Activate	0.077	0.39	W
	DDR–RD/WR/Term	0.115	1.20	W
	Power Supplies		TBD	W
	Other		TBD	W
	———————-	———	———	
	Total		**8.35+**	W

DDR memory access limited to 10% and an FPGA design that is not pushing F_{MAX}, such as running most of the logic at 100MHz and I/O pins running 50 to 100MHz.

Table 31: MitySOM-5CSE Power Ranges

SOM	Subsystem	Minimum [32]	Maximum	UNIT
5CSE-S2-3XA	Static HPS	0.017	0.08	W
	HPS		1.04	W
	Static FPGA Fabric	0.301	0.35	W
	FPGA		0.81	W
	GXB	0	0	W
	PCS and HIP	0	0	W
	DDR–Background	0.265	0.28	W
	DDR–Activate	0.080	0.76	W
	DDR–RD/WR/Term	0.230	0.84	W
	Power Supplies		TBD	W
	Other		TBD	W
	———————-	———	———	
	Total		**4.16+**	W
5CSE-L2-3YA	Static HPS	0.017	0.08	W
	HPS	1.00 ??	1.04	W
	Static FPGA Fabric	0.301	0.35	W
	FPGA	0.20 ??	0.81	W
	GXB	0	0	W
	PCS and HIP	0	0	W
	DDR–Background	0.106	0.11	W
	DDR–Activate	0.032	0.23	W
	DDR–RD/WR/Term	0.092	0.26	W
	Power Supplies	0.092	0.15	W
	Other		TBD	W
	———————-	———	———	
	Total	**1.75+**	**3.03+**	W

9 Document Revision History

Date	Version	Change Description
16-Jul-2014	1.0	Initial version
10-Nov-2014	1.1	Added MitySOM-5CSE Variants
12-Jan-2015	1.2	Corrected Expanded I/O pins for B5A-TX-R3 in Table 27. Added pin migration details across MitySOM-5CSx family of modules. Updated Ext Interface Figure 2 to color-code Expanded I/O signal group.
31-Mar-2015	1.3	Updated Altera links. Added external link to MSEL configuration details.