

## Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use <http://www.nexperia.com>

Instead of [sales.addresses@www.nxp.com](mailto:sales.addresses@www.nxp.com) or [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com), use [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com) (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

# 74AHC126; 74AHCT126

Quad buffer/line driver; 3-state

Rev. 04 — 12 August 2009

Product data sheet

## 1. General description

---

The 74AHC126; 74AHCT126 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC126; 74AHCT126 provides four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW-level at pin nOE causes the outputs to assume a high-impedance OFF-state.

The 74AHC126; 74AHCT126 is identical to the 74AHC125; 74AHCT125 but has active HIGH output enable inputs.

## 2. Features

---

- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Inputs accept voltages higher than  $V_{CC}$
- Input levels:
  - ◆ For 74AHC126: CMOS level
  - ◆ For 74AHCT126: TTL level
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AHC126D 74AHCT126D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHC126PW 74AHCT126PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHC126BQ 74AHCT126BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

### 4. Functional diagram

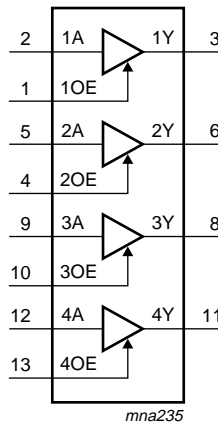


Fig 1. Functional diagram

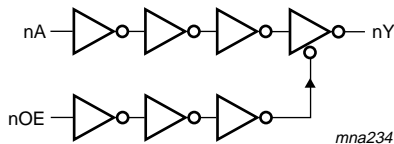


Fig 2. Logic symbol

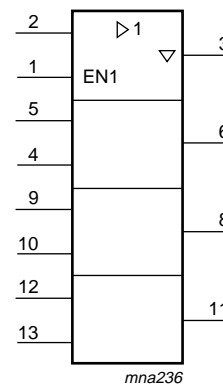
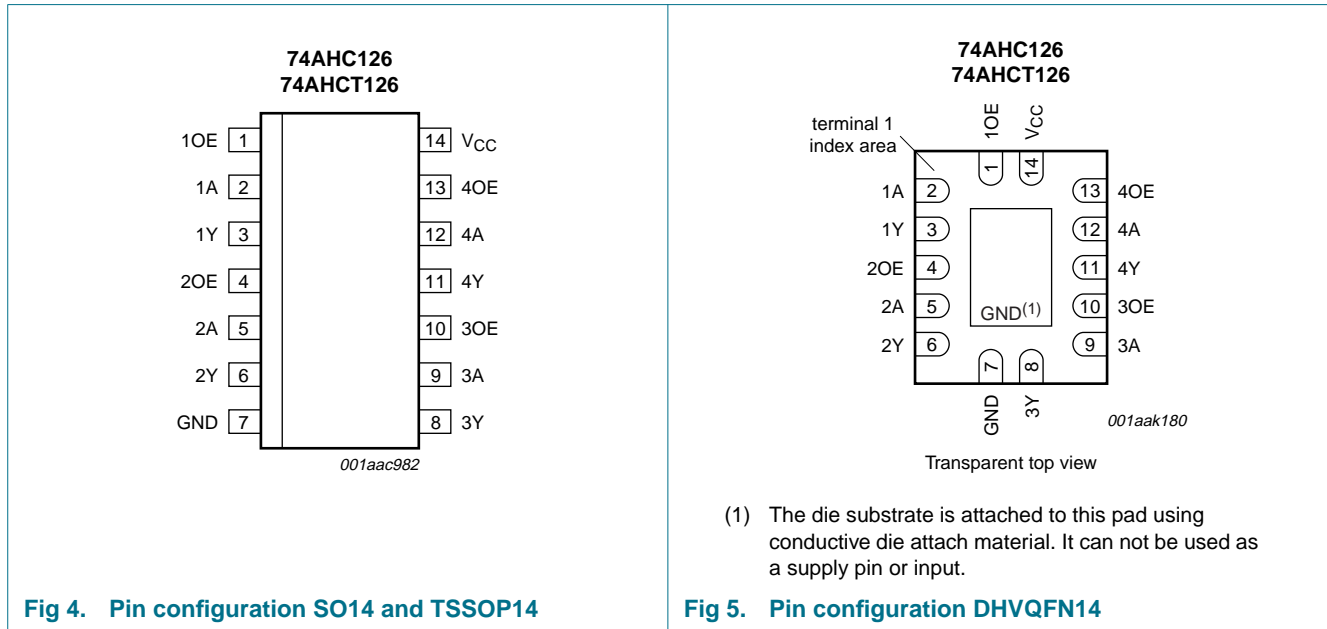


Fig 3. IEC logic symbol

## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Description
10E	1	output enable input 1 (active HIGH)
1A	2	data input 1
1Y	3	data output 1
2OE	4	output enable input 2 (active HIGH)
2A	5	data input 2
2Y	6	data output 2
GND	7	ground (0 V)
3Y	8	data output 3
3A	9	data input 3
3OE	10	output enable input 3 (active HIGH)
4Y	11	data output 4
4A	12	data input 4
4OE	13	output enable input 4 (active HIGH)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3.** Function table<sup>[1]</sup>

Control	Input	Output
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

- [1] H = HIGH voltage state;  
 L = LOW voltage state;  
 X = don't care;  
 Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4.** Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	<sup>[1]</sup> -20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	<sup>[1]</sup> -20	+20	mA
$I_O$	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-25	+25	mA
$I_{CC}$	supply current		-	+75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	<sup>[2]</sup> -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] For SO14 packages: above 70 °C the value of  $P_{tot}$  derates linearly at 8 mW/K.  
 For TSSOP14 packages: above 60 °C the value of  $P_{tot}$  derates linearly at 5.5 mW/K.  
 For DHVQFN14 packages: above 60 °C the value of  $P_{tot}$  derates linearly at 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>74AHC126</b>						
$V_{CC}$	supply voltage		2.0	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	100	ns/V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	20	ns/V
<b>74AHCT126</b>						
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC126</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	-	-	1.5	-	1.5	-	V
		$V_{CC} = 3.0\text{ V}$	2.1	-	-	2.1	-	2.1	-	V
		$V_{CC} = 5.5\text{ V}$	3.85	-	-	3.85	-	3.85	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	-	0.5	-	0.5	-	0.5	V
		$V_{CC} = 3.0\text{ V}$	-	-	0.9	-	0.9	-	0.9	V
		$V_{CC} = 5.5\text{ V}$	-	-	1.65	-	1.65	-	1.65	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -50\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50\ \mu\text{A}; V_{CC} = 3.0\text{ V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0\text{ mA}; V_{CC} = 3.0\text{ V}$	2.58	-	-	2.48	-	2.40	-	V
	$I_O = -8.0\text{ mA}; V_{CC} = 4.5\text{ V}$	3.94	-	-	3.80	-	3.70	-	V	
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 50\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50\ \mu\text{A}; V_{CC} = 3.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.36	-	0.44	-	0.55	V
	$I_O = 8.0\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.36	-	0.44	-	0.55	V	

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	$\pm 0.25$	-	$\pm 2.5$	-	$\pm 10.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	$\mu\text{A}$
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
$C_O$	output capacitance		-	4	-	-	-	-	-	pF

### 74AHCT126

$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$ $I_O = -50 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$ $I_O = 50 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND per input pin; other inputs at $V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	$\pm 0.25$	-	$\pm 2.5$	-	$\pm 10.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; other pins at $V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
$C_O$	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

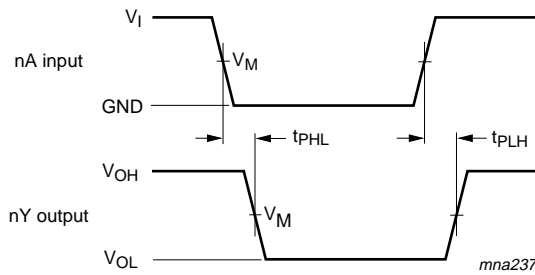
Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
<b>74AHC126</b>										
t <sub>pd</sub>	propagation delay	nA to nY; see Figure 6 <sup>[2]</sup>								
		V <sub>CC</sub> = 3.0 V to 3.6 V								
		C <sub>L</sub> = 15 pF	-	4.7	8.0	1.0	9.5	1.0	10.0	ns
		C <sub>L</sub> = 50 pF	-	6.7	11.5	1.0	13.0	1.0	14.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	3.3	5.5	1.0	6.5	1.0	7.0	ns
		C <sub>L</sub> = 50 pF	-	4.7	7.5	1.0	8.5	1.0	9.5	ns
t <sub>en</sub>	enable time	nOE to nY; see Figure 7 <sup>[3]</sup>								
		V <sub>CC</sub> = 3.0 V to 3.6 V								
		C <sub>L</sub> = 15 pF	-	5.3	8.0	1.0	9.5	1.0	10.0	ns
		C <sub>L</sub> = 50 pF	-	7.6	11.5	1.0	13.0	1.0	14.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	3.6	5.3	1.0	6.1	1.0	7.0	ns
		C <sub>L</sub> = 50 pF	-	5.1	7.6	1.0	8.7	1.0	9.5	ns
t <sub>dis</sub>	disable time	nOE to nY; see Figure 7 <sup>[4]</sup>								
		V <sub>CC</sub> = 3.0 V to 3.6 V								
		C <sub>L</sub> = 15 pF	-	6.6	9.7	1.0	11.5	1.0	12.5	ns
		C <sub>L</sub> = 50 pF	-	9.4	13.2	1.0	15.0	1.0	16.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	4.7	6.8	1.0	8.0	1.0	8.5	ns
		C <sub>L</sub> = 50 pF	-	6.7	8.8	1.0	10.0	1.0	11.0	ns
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[5]</sup>	-	10	-	-	-	-	-	pF
<b>74AHCT126; V<sub>CC</sub> = 4.5 V to 5.5 V</b>										
t <sub>pd</sub>	propagation delay	nA to nY; see Figure 6 <sup>[2]</sup>								
		C <sub>L</sub> = 15 pF	-	3.0	5.5	1.0	6.5	1.0	7.0	ns
		C <sub>L</sub> = 50 pF	-	4.3	7.5	1.0	8.5	1.0	9.5	ns
t <sub>en</sub>	enable time	nOE to nY; see Figure 7 <sup>[3]</sup>								
		C <sub>L</sub> = 15 pF	-	3.3	5.1	1.0	6.0	1.0	6.5	ns
		C <sub>L</sub> = 50 pF	-	4.7	7.1	1.0	8.0	1.0	9.0	ns
t <sub>dis</sub>	disable time	nOE to nY; see Figure 7 <sup>[4]</sup>								
		C <sub>L</sub> = 15 pF	-	4.8	6.8	1.0	8.0	1.0	8.5	ns
		C <sub>L</sub> = 50 pF	-	6.9	8.9	1.0	10.0	1.0	11.5	ns
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[5]</sup>	-	12	-	-	-	-	-	pF



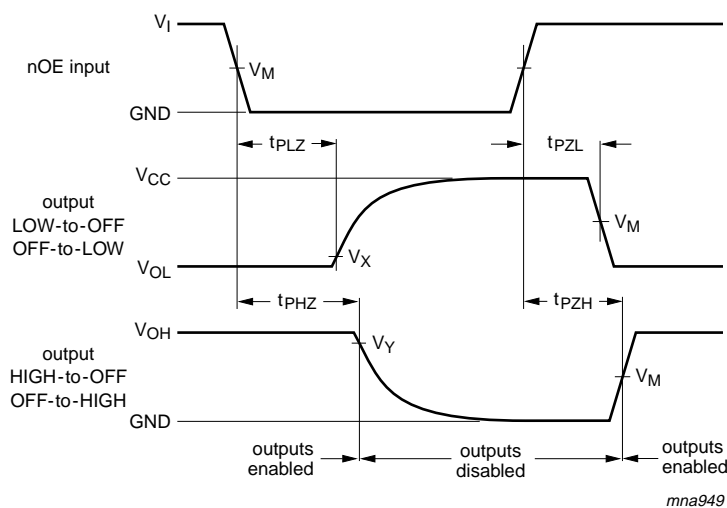
- [1] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 5.0\text{ V}$ ).
- [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [3]  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .
- [4]  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .
- [5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in V;  
 $N$  = number of inputs switching;  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## 11. Waveforms



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. Input to output propagation delays**

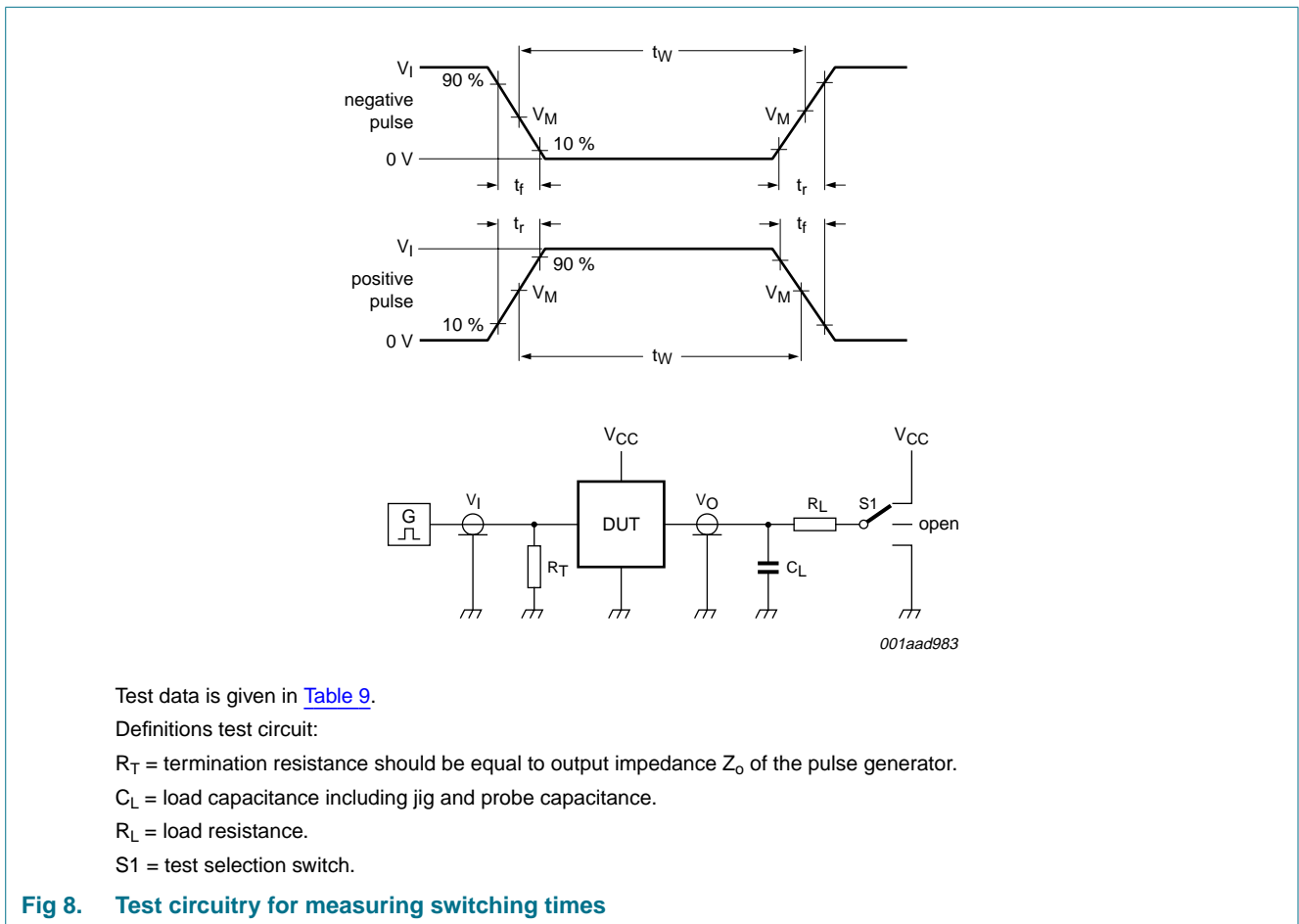


Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Enable and disable times**

**Table 8. Measurement points**

Type	Input		Output	
	$V_M$	$V_M$	$V_X$	$V_Y$
74AHC126	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
74AHCT126	1.5 V	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



**Fig 8. Test circuitry for measuring switching times**

**Table 9. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74AHC126	$V_{CC}$	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74AHCT126	3.0 V	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

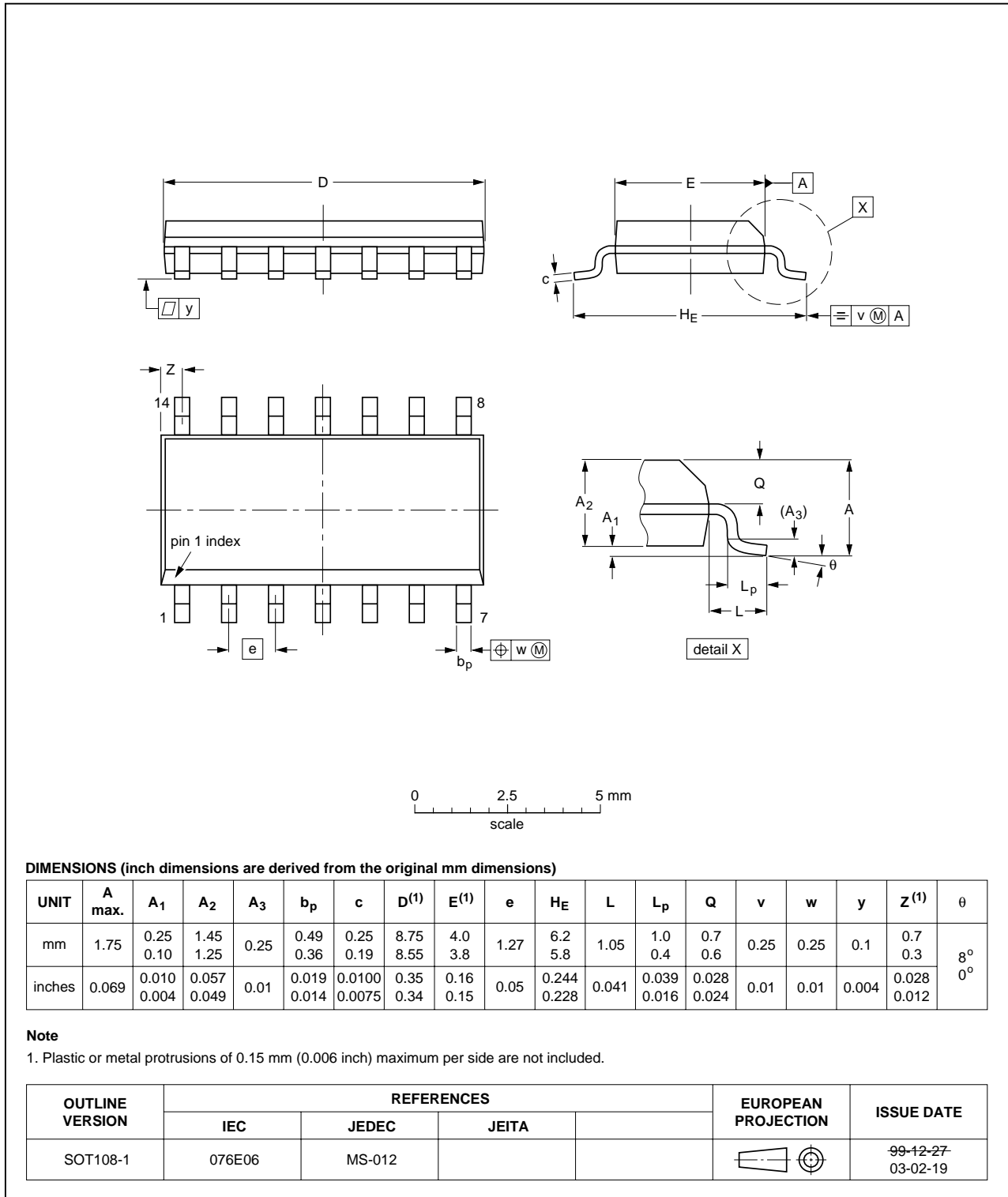


Fig 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

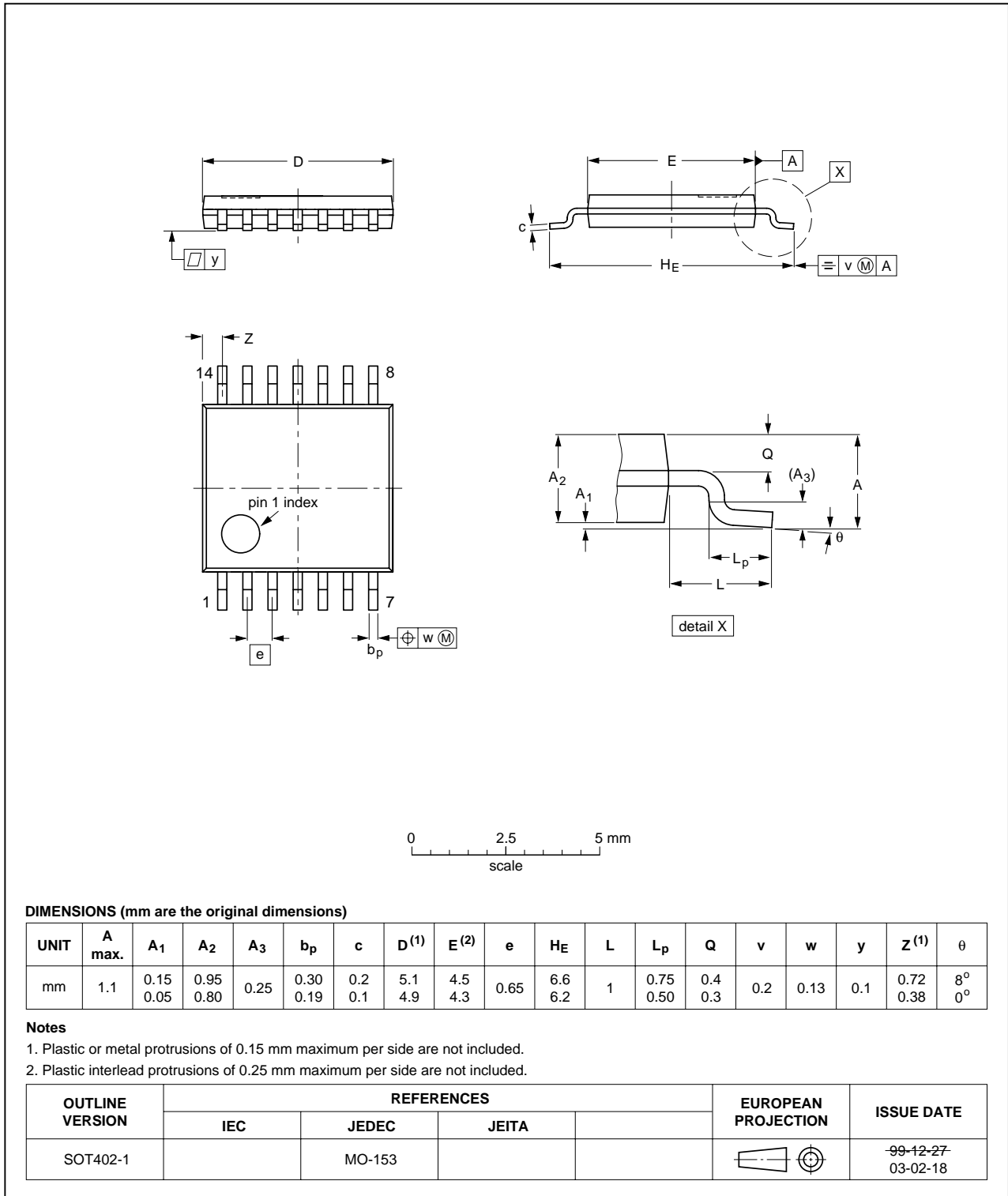
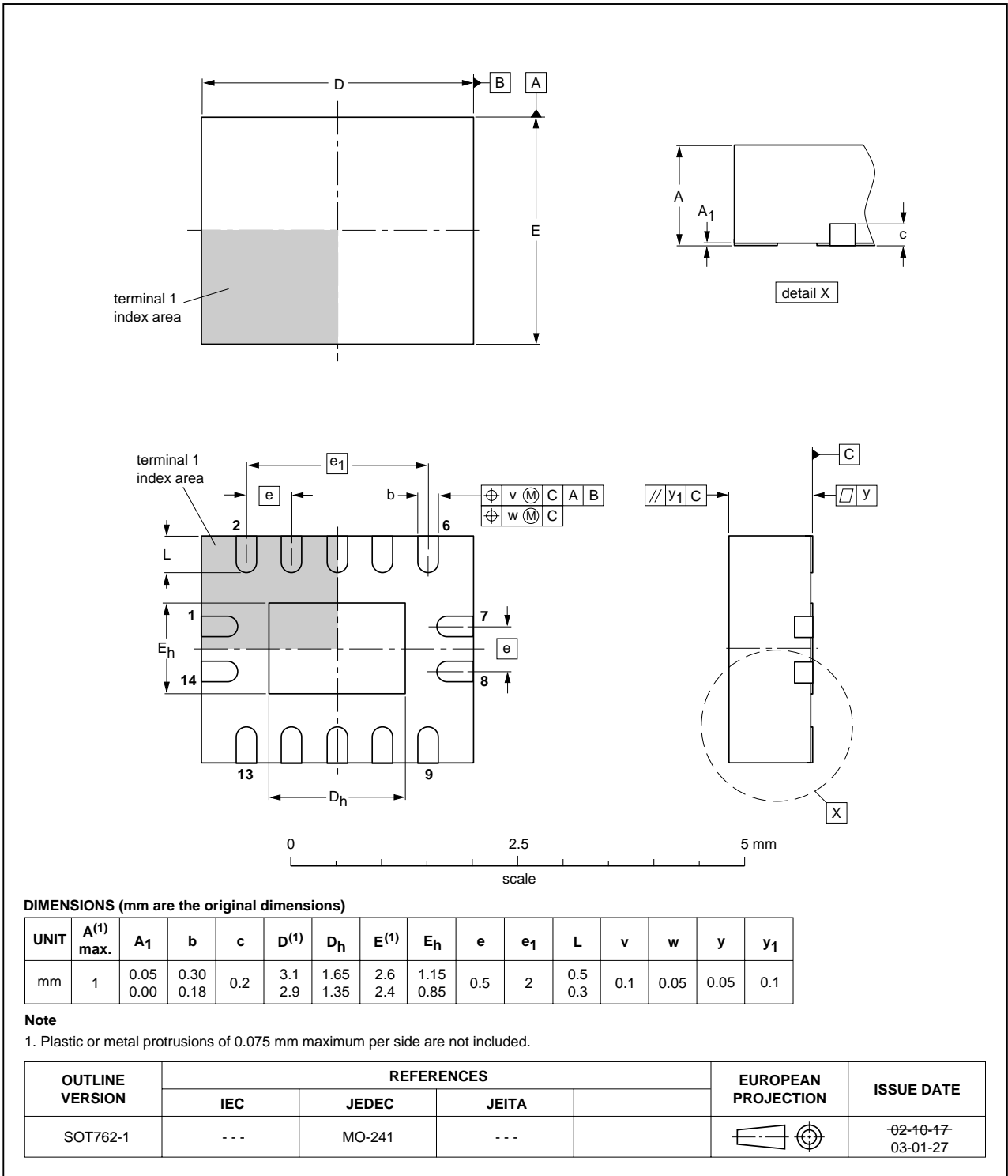


Fig 10. Package outline SOT402-1 (TSSOP14)

**DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm**

**SOT762-1**



**Fig 11. Package outline SOT762-1 (DHVQFN14)**

## 13. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT126_4	20090812	Product data sheet	-	74AHC_AHCT126_3
Modifications:	<ul style="list-style-type: none"> <li>Added type numbers 74AHC126BQ and 74AHCT126BQ (DHVQFN14 package)</li> </ul>			
74AHC_AHCT126_3	20080425	Product data sheet	-	74AHC_AHCT126_2
74AHC_AHCT126_2	19990929	Product specification	-	74AHC_AHCT126_N_1
74AHC_AHCT126_N_1	19990112	Preliminary specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 15.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

### 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 17. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>3</b>
5.1	Pinning .....	3
5.2	Pin description .....	3
<b>6</b>	<b>Functional description</b> .....	<b>4</b>
<b>7</b>	<b>Limiting values</b> .....	<b>4</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>5</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>5</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>7</b>
<b>11</b>	<b>Waveforms</b> .....	<b>8</b>
<b>12</b>	<b>Package outline</b> .....	<b>10</b>
<b>13</b>	<b>Abbreviations</b> .....	<b>13</b>
<b>14</b>	<b>Revision history</b> .....	<b>13</b>
<b>15</b>	<b>Legal information</b> .....	<b>14</b>
15.1	Data sheet status .....	14
15.2	Definitions .....	14
15.3	Disclaimers .....	14
15.4	Trademarks .....	14
<b>16</b>	<b>Contact information</b> .....	<b>14</b>
<b>17</b>	<b>Contents</b> .....	<b>15</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2009.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 12 August 2009

Document identifier: 74AHC\_AHCT126\_4