TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VHC165F, TC74VHC165FT, TC74VHC165FK

## 8-Bit Shift Register (P-IN, S-OUT)

The TC74VHC165 is an advanced high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate $C^2MOS$ technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

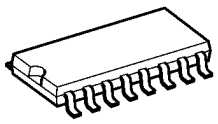
It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock input. When the SHIFT/$\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight frip-frops perform serial shifting with each clock pulse.

When the SHIFT/$\overline{\text{LOAD}}$ input is held low, the parallel data is loaded synchronously into the register at positive going transition of the clock pulse.

The CK-INH input should be shifted high only when the CK input is held high.

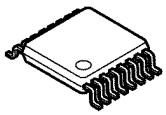
An Input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

TC74VHC165F



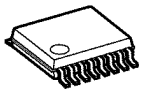
SOP16-P-300-1.27A

TC74VHC165FT



TSSOP16-P-0044-0.65A

TC74VHC165FK



VSSOP16-P-0030-0.50

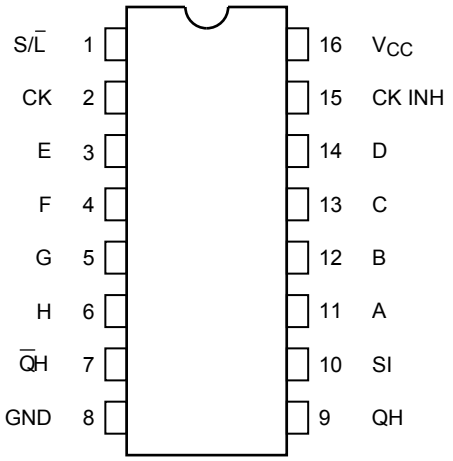
Weight
SOP16-P-300-1.27A: 0.18 g (typ.)
TSSOP16-P-0044-0.65A: 0.06 g (typ.)
VSSOP16-P-0030-0.50: 0.02 g (typ.)

## Features

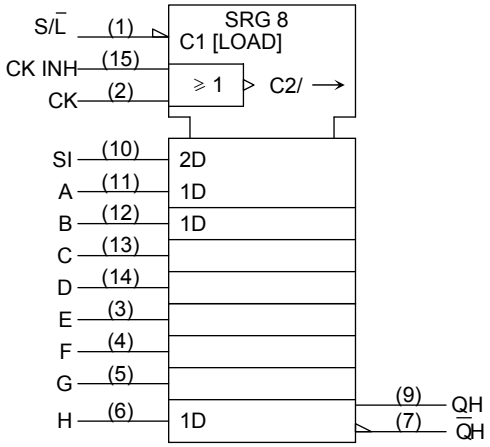
- High speed: $f_{max}$ = 150 MHz (typ.) at $V_{CC}$ = 5 V
- Low power dissipation: $I_{CC}$ = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$ (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: $V_{CC}$ (opr) = 2 V to 5.5 V
- Pin and function compatible with 74ALS165

Start of commercial production
1992-05

## Pin Assignment




## IEC Logic Symbol




## Truth Table

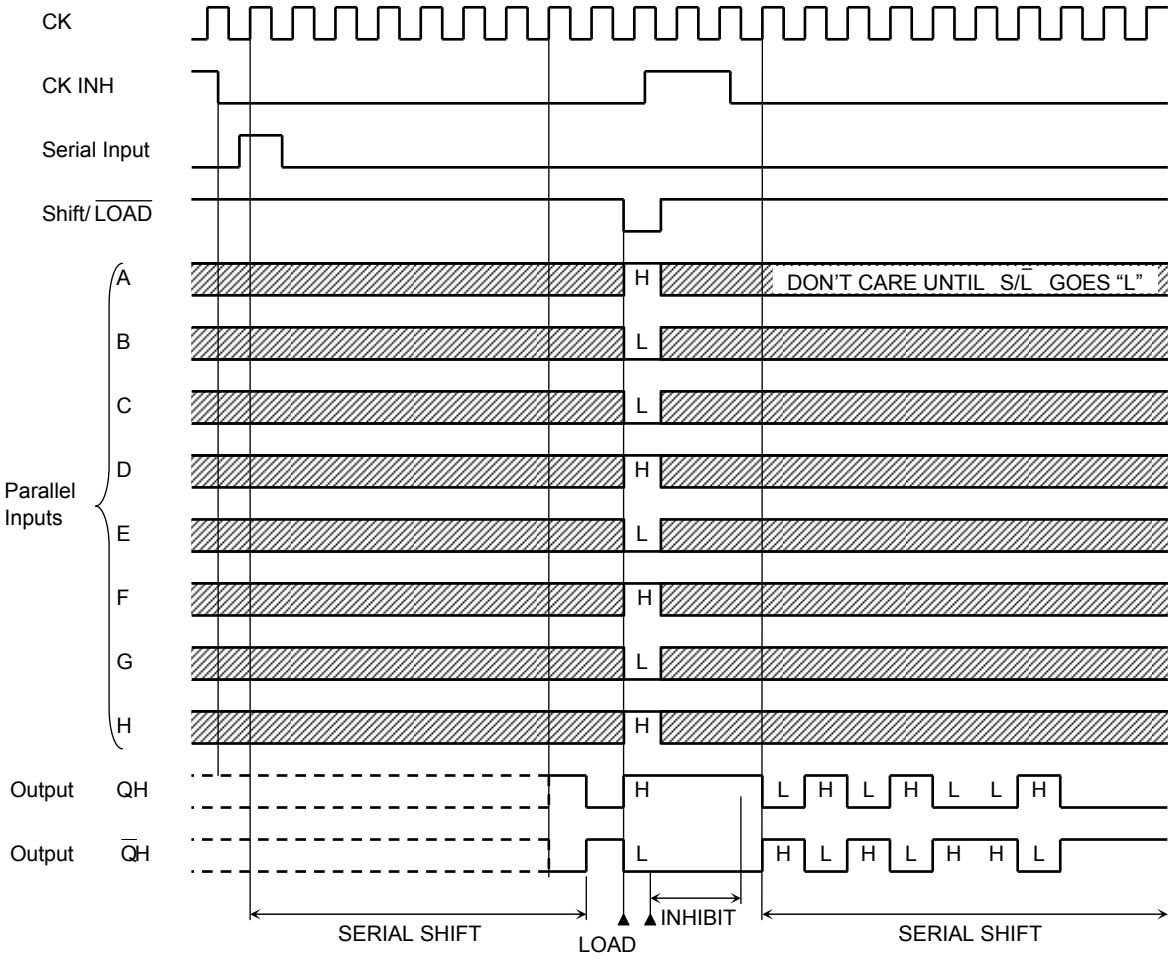
| Inputs | | | | | Internal Outputs | | Outputs | |
|---|---|---|---|---|---|---|---|---|
| SHIFT/$\overline{LOAD}$ | CK INH | CK | SERIAL IN | PARALLEL A·····H | QA | QB | QH | $\overline{Q}$H |
| L | X | X | X | a·····h | a | b | h | $\overline{h}$ |
| H | L | ↑ | H | X | H | $QA_n$ | $QG_n$ | $\overline{Q}G_n$ |
| H | L | ↑ | L | X | L | $QA_n$ | $QG_n$ | $\overline{Q}G_n$ |
| H | ↑ | L | H | X | H | $QA_n$ | $QG_n$ | $\overline{Q}G_n$ |
| H | ↑ | L | L | X | L | $QA_n$ | $QG_n$ | $\overline{Q}G_n$ |
| H | X | H | X | X | No Change | | | |
| H | H | X | X | X | No Change | | | |

X: Don't care

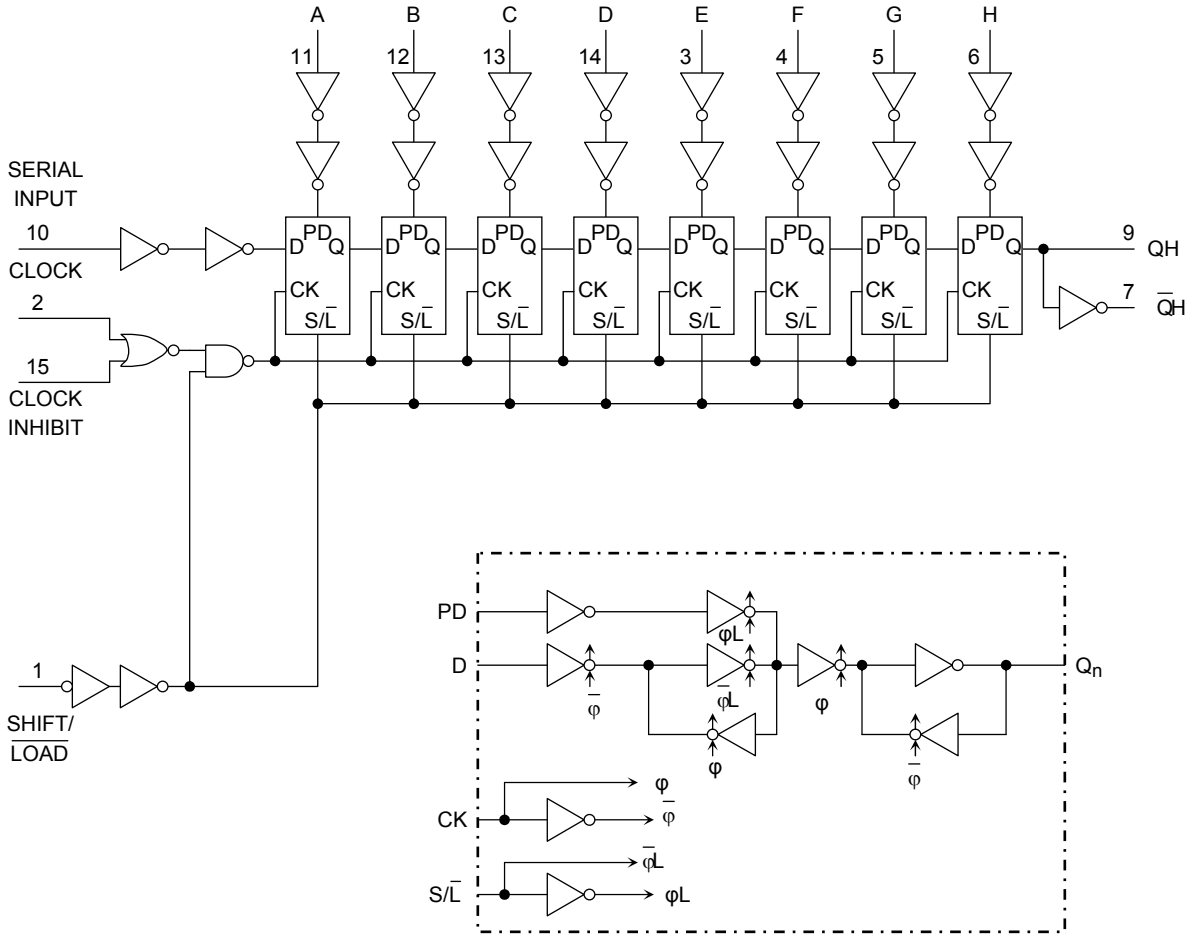
a·····h: The level of steady state input voltage at inputs A through H respectively

$QA_n$ to $QG_n$: The level of QA to QG, respectively, before the most recent positive transition of the CK.

## Timing Chart



## System Diagram




## Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | $V_{CC}$ | −0.5 to 7.0 | V |
| DC input voltage | $V_{IN}$ | −0.5 to 7.0 | V |
| DC output voltage | $V_{OUT}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| Input diode current | $I_{IK}$ | −20 | mA |
| Output diode current | $I_{OK}$ | ±20 | mA |
| DC output current | $I_{OUT}$ | ±25 | mA |
| DC $V_{CC}$/ground current | $I_{CC}$ | ±50 | mA |
| Power dissipation | $P_D$ | 180 | mW |
| Storage temperature | $T_{stg}$ | −65 to 150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2.0 to 5.5 | V |
| Input voltage | $V_{IN}$ | 0 to 5.5 | V |
| Output voltage | $V_{OUT}$ | 0 to $V_{CC}$ | V |
| Operating temperature | $T_{opr}$ | −40 to 85 | °C |
| Input rise and fall time | dt/dv | 0 to 100 ($V_{CC}$ = 3.3 ± 0.3 V)<br>0 to 20 ($V_{CC}$ = 5 ± 0.5 V) | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either $V_{CC}$ or GND.

## Electrical Characteristics

### DC Characteristics

| Characteristics | Symbol | Test Condition | | Ta = 25°C | | | Ta = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | Min | Typ. | Max | Min | Max | |
| High-level input voltage | $V_{IH}$ | — | 2.0 | 1.50 | — | — | 1.50 | — | V |
| | | | 3.0 to 5.5 | $V_{CC}$ × 0.7 | — | — | $V_{CC}$ × 0.7 | — | |
| Low-level input voltage | $V_{IL}$ | — | 2.0 | — | — | 0.50 | — | 0.50 | V |
| | | | 3.0 to 5.5 | — | — | $V_{CC}$ × 0.3 | — | $V_{CC}$ × 0.3 | |
| High-level output voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −50 μA | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | 3.0 | 2.9 | 3.0 | — | 2.9 | — | |
| | | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | |
| | | | $I_{OH}$ = −4 mA | 3.0 | 2.58 | — | — | 2.48 | — | |
| | | | $I_{OH}$ = −8 mA | 4.5 | 3.94 | — | — | 3.80 | — | |
| Low-level output voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 3.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 3.0 | — | — | 0.36 | — | 0.44 | |
| | | | $I_{OL}$ = 8 mA | 4.5 | — | — | 0.36 | — | 0.44 | |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = 5.5 V or GND | | 0 to 5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | 4.0 | — | 40.0 | μA |

**Timing Requirements (input: $t_r = t_f = 3$ ns)**

| Characteristics | Symbol | Test Condition | | Ta = 25°C | Ta = −40 to 85°C | Unit |
|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | Limit | Limit | |
| Minimum pulse width (CK, CK INH) | $t_{w\,(L)}$<br>$t_{w\,(H)}$ | — | 3.3 ± 0.3<br>5.0 ± 0.5 | 6.0<br>4.0 | 7.0<br>4.0 | ns |
| Minimum pulse width ( $\overline{S/L}$ ) | $t_{w\,(L)}$ | — | 3.3 ± 0.3<br>5.0 ± 0.5 | 7.5<br>5.0 | 9.0<br>6.0 | ns |
| Minimum set-up time (PI- $\overline{S/L}$ ) | $t_s$ | — | 3.3 ± 0.3<br>5.0 ± 0.5 | 7.5<br>5.0 | 8.5<br>5.0 | ns |
| Minimum set-up time (SI-CK, CK INH) | $t_s$ | — | 3.3 ± 0.3<br>5.0 ± 0.5 | 5.0<br>4.0 | 6.0<br>4.0 | ns |
| Minimum set-up time ( $\overline{S/L}$ -CK, CK INH) | $t_s$ | — | 3.3 ± 0.3<br>5.0 ± 0.5 | 5.0<br>4.0 | 6.0<br>4.0 | ns |
| Minimum hold time (PI- $\overline{S/L}$ ) | $t_h$ | — | 3.3 ± 0.3<br>5.0 ± 0.5 | 0.5<br>1.0 | 0.5<br>1.0 | ns |
| Minimum hold time (SI-CK, CK INH) | $t_h$ | — | 3.3 ± 0.3<br>5.0 ± 0.5 | 0.0<br>0.5 | 0.0<br>0.5 | ns |
| Minimum hold time ( $\overline{S/L}$ -CK, CK INH) | $t_h$ | — | 3.3 ± 0.3<br>5.0 ± 0.5 | 0.0<br>0.5 | 0.0<br>0.5 | ns |
| Minimum removal time (CK INH-CK) (CK-CK INH) | $t_{rem}$ | — | 3.3 ± 0.3<br>5.0 ± 0.5 | 5.0<br>3.5 | 5.0<br>3.5 | ns |

**AC Characteristics (input: $t_r = t_f = 3$ ns)**

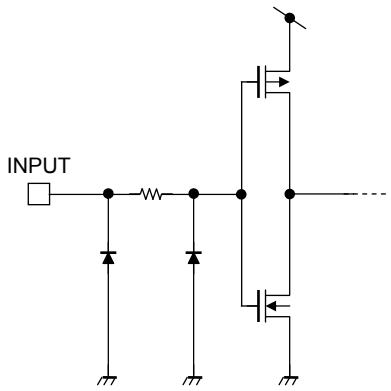
| Characteristics | Symbol | Test Condition | | | Ta = 25°C | | | Ta = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | $C_L$ (pF) | Min | Typ. | Max | Min | Max | |
| Propagation delay time (CK, CK INH-QH, $\overline{QH}$) | $t_{pLH}$ $t_{pHL}$ | — | 3.3 ± 0.3 | 15 | — | 9.9 | 15.4 | 1.0 | 18.0 | ns |
| | | | | 50 | — | 12.4 | 18.9 | 1.0 | 21.5 | |
| | | | 5.0 ± 0.5 | 15 | — | 6.6 | 9.9 | 1.0 | 11.5 | |
| | | | | 50 | — | 8.1 | 11.9 | 1.0 | 13.5 | |
| Propagation delay time ($S/\overline{L}$-QH, $\overline{QH}$) | $t_{pLH}$ $t_{pHL}$ | — | 3.3 ± 0.3 | 15 | — | 9.9 | 15.8 | 1.0 | 18.5 | ns |
| | | | | 50 | — | 12.4 | 19.3 | 1.0 | 22.0 | |
| | | | 5.0 ± 0.5 | 15 | — | 6.7 | 9.9 | 1.0 | 11.5 | |
| | | | | 50 | — | 8.2 | 11.9 | 1.0 | 13.5 | |
| Propagation delay time (H-QH, $\overline{QH}$) | $t_{pLH}$ $t_{pHL}$ | — | 3.3 ± 0.3 | 15 | — | 9.2 | 14.1 | 1.0 | 16.5 | ns |
| | | | | 50 | — | 11.7 | 17.6 | 1.0 | 20.0 | |
| | | | 5.0 ± 0.5 | 15 | — | 5.9 | 9.0 | 1.0 | 10.5 | |
| | | | | 50 | — | 7.4 | 11.0 | 1.0 | 12.5 | |
| Maximum clock frequency | $f_{max}$ | — | 3.3 ± 0.3 | 15 | 65 | 85 | — | 55 | — | MHz |
| | | | | 50 | 60 | 105 | — | 50 | — | |
| | | | 5.0 ± 0.5 | 15 | 110 | 150 | — | 90 | — | |
| | | | | 50 | 95 | 130 | — | 85 | — | |
| Input capacitance | $C_{IN}$ | — | | | — | 4 | 10 | — | 10 | pF |
| Power dissipation capacitance | $C_{PD}$ | (Note) | | | — | 50 | — | — | — | pF |

Note: $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

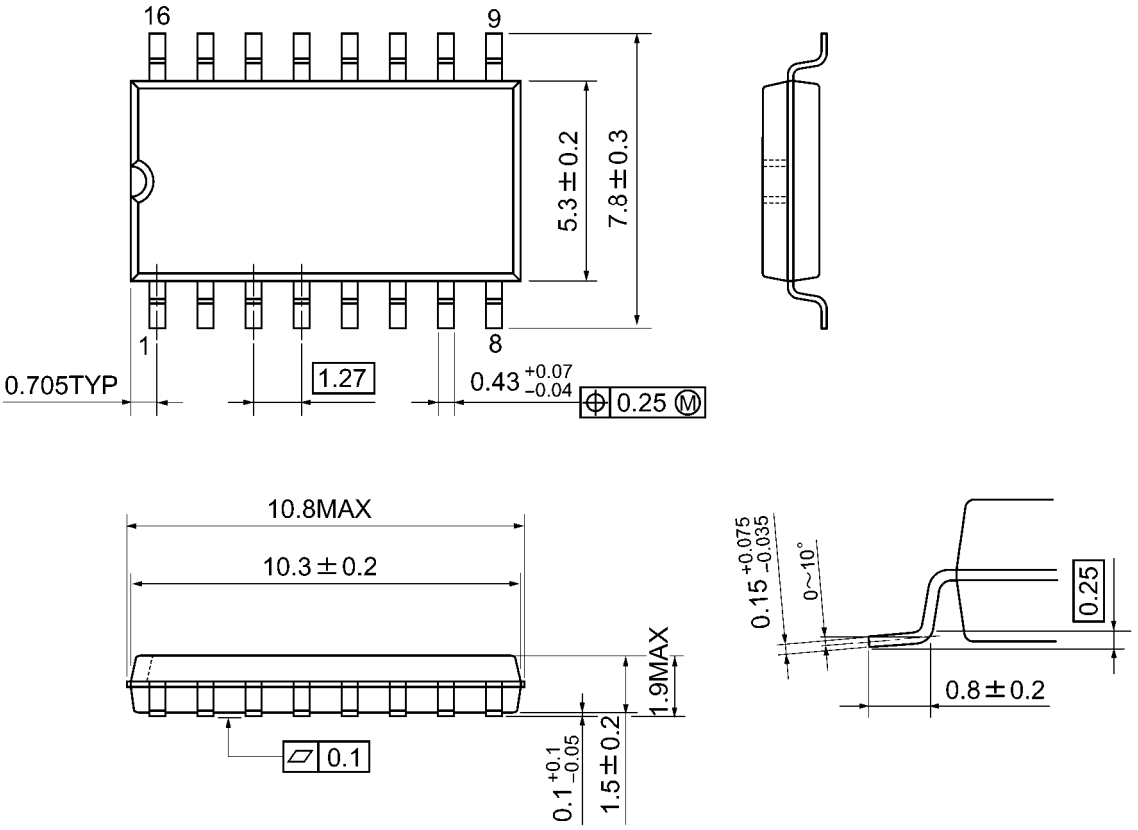
$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

## Input Equivalent Circuit



## Package Dimensions

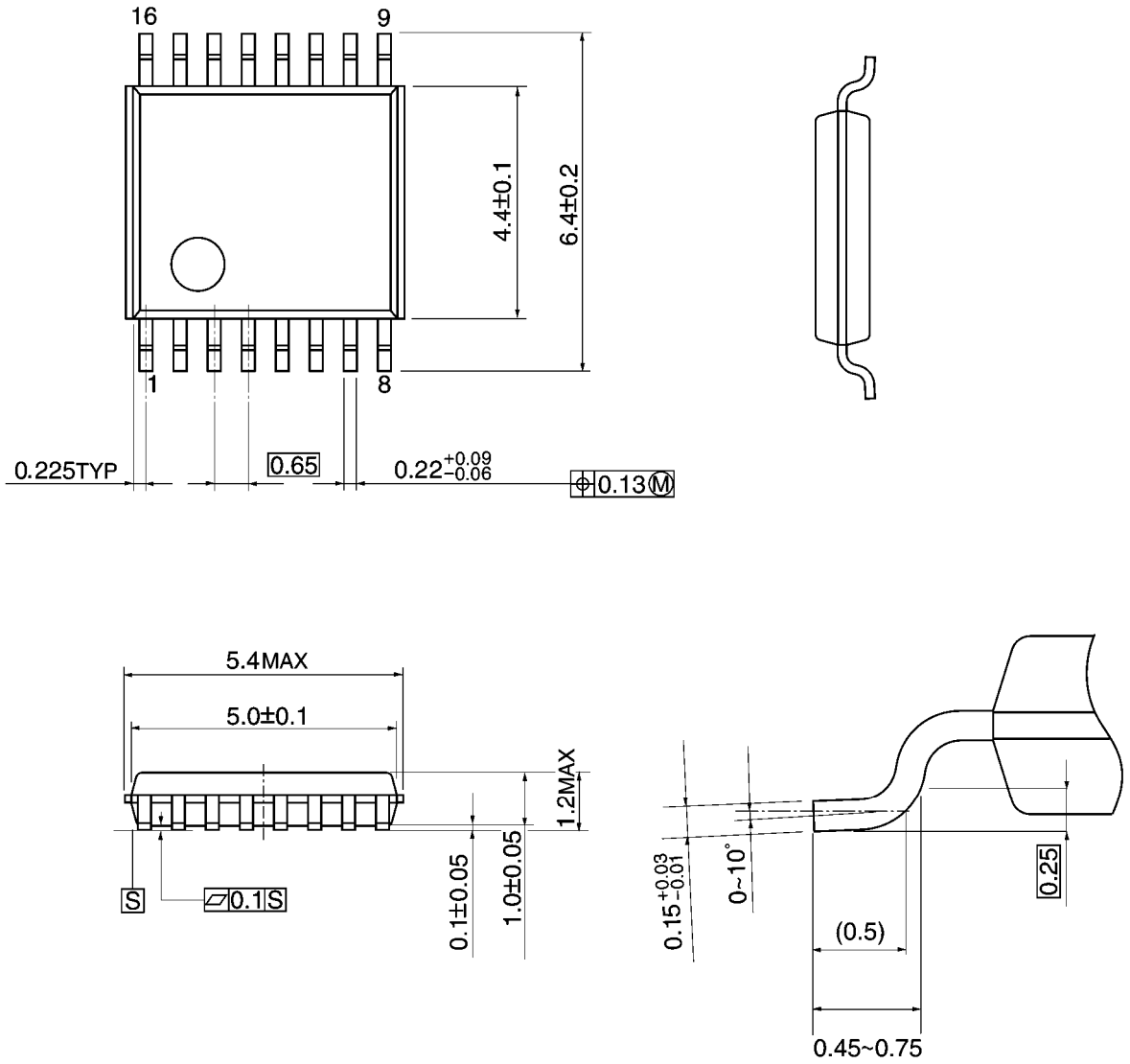
SOP16-P-300-1.27A Unit: mm




Weight: 0.18 g (typ.)

## Package Dimensions

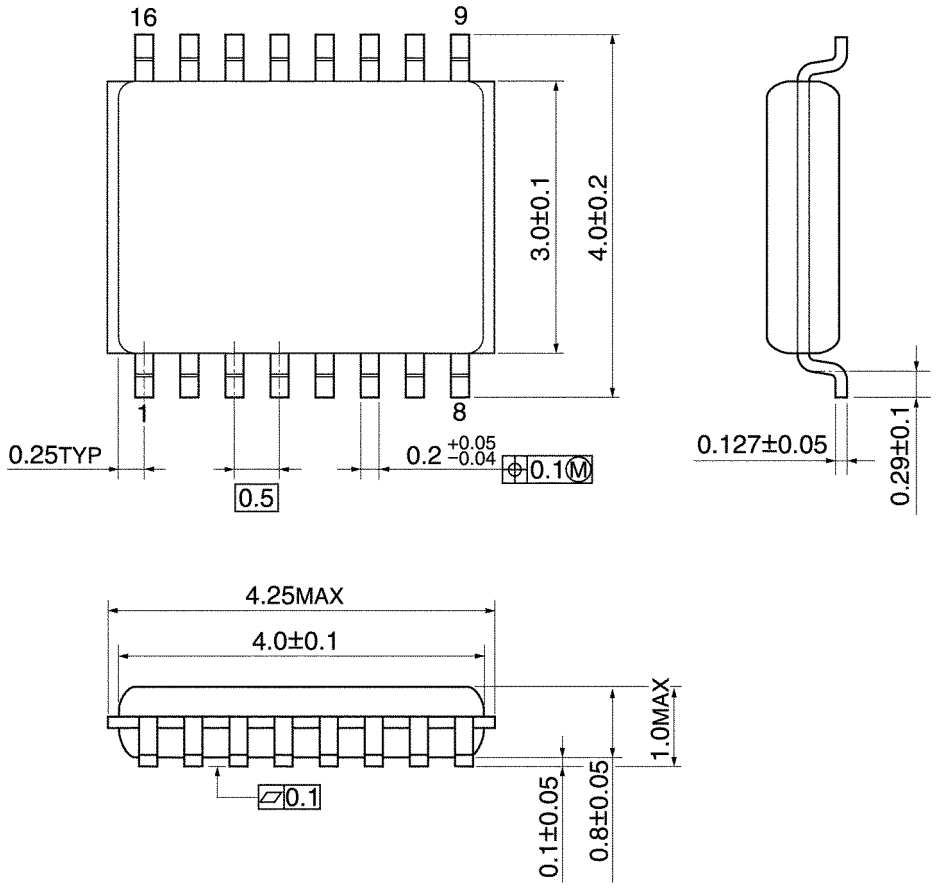
TSSOP16-P-0044-0.65A Unit: mm




Weight: 0.06 g (typ.)

## Package Dimensions

VSSOP16-P-0030-0.50 Unit: mm




Weight: 0.02 g (typ.)

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