ENC424J600/624J600

ENC424J600/624J600 Silicon Errata and Data Sheet Clarification

The ENC424J600/624J600 devices that you have received conform functionally to the current Device Data Sheet (DS39935**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the combined Device/Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be retrieved by querying the read-only EIDLEDL register (when using one of the 8-bit interfaces) or the lower byte of the EIDLED register (when using a 16-bit interface). Please refer to the Device Data Sheet for detailed information on accessing these registers.

The values for the various ENC424J600/624J600 silicon revisions are shown in Table 1.

TABLE 1: COMBINED DEVICE/REVISION ID

Part Number	Value of EIDLEDL or EIDLED<7:0>
	A2
ENC424J600	21h
ENC624J600	

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A2
PHY	Receive	1.	Rare packet loss following collisions, 10Base-T Half-Duplex mode	X
PHY	Transmit	2.	Deviations from MAU Eye Pattern in 10Base-T mode	X
PHY	Transmit	3.	Rise time/fall time asymmetry in MLT3 signal	X
Memory	SFR	4.	CRYPTEN bit cannot be changed by BFC/BFS/BFCU/BFSU opcodes or EIRSET/EIRCLR registers.	X
AES	—	5.	AES module produces incorrect results.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: PHY (Receive)

On rare occasions, in 10Base-T Half-Duplex mode, a collision will cause the immediately following packet to be received incorrectly. This causes the packet to be dropped. This condition may occur on an average of one to four times per 10,000 collisions.

Full-Duplex mode and 100Base-TX modes are unaffected by this issue. Typical modern networks are deployed using Ethernet switching technology and will not experience any collisions or packet loss due to this issue. In the uncommon case that an affected network infrastructure is used, upper layer communications protocols, such as TCP, will normally perform automatic retransmission to ensure that no application data is lost.

Work around

None.

Affected Silicon Revisions

A2							
X							

2. Module: PHY (Transmit)

When transmitting random data in 10Base-T mode, the PHY transmit waveform slightly violates the MAU eye diagram keep-out zones specified in the IEEE 802.3™ Std. 2005, Section 14.3.1.2.1. Specifically, the waveform amplitude is slightly too high for '0' to '1' and '1' to '0' bit transitions when tested against the twisted-pair model, as shown in Figure 1.

This issue applies only to 10 Mbps speed and is unlikely to cause compatibility problems in real networks. When terminated with a 100Ω resistor without the twisted-pair model, the transmit waveform stays within the amplitude limits of +2.2V to +2.8V and -2.2V to -2.8V required by the standard.

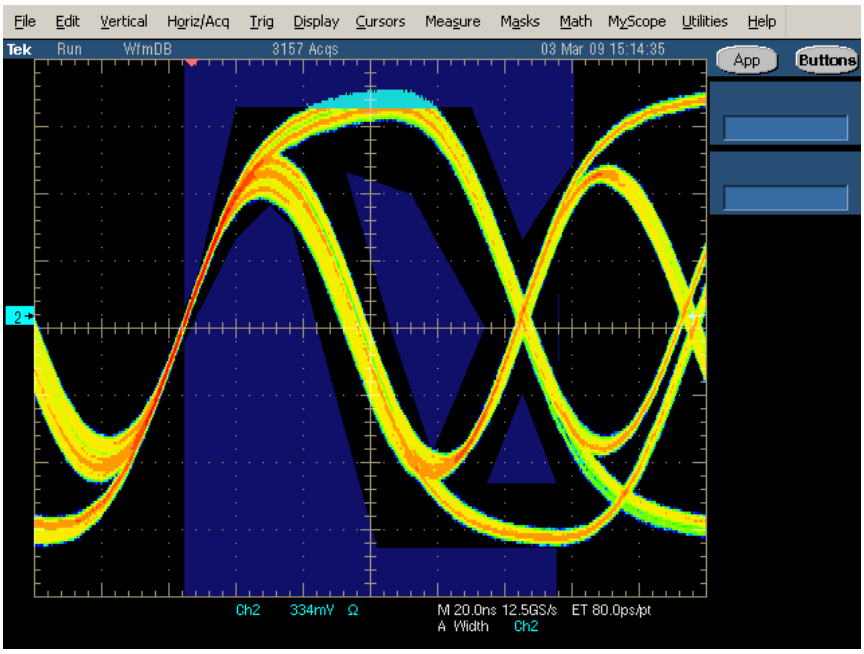
Work around

None.

Affected Silicon Revisions

A2							
X							

FIGURE 1: 10Base-T MAU EYE DIAGRAM



3. Module: PHY (Transmit)

For 100Base-TX operation, the IEEE 802.3 specification requires the rise and fall times of the MLT3 signal to match within 0.5 ns, measured over 10 different intervals. The actual rise/fall time symmetry measurements may occasionally be slightly above this level.

This issue has no substantial impact on the quality of the transmitted signal and will not impact applications operating in real networks.

Work around

None.

Affected Silicon Revisions

A2							
X							

4. Module: Memory (SFR)

The CRYPTEN bit (EIR<15>) cannot be changed using the Bit Field Set (BFS), Bit Field Clear (BFC), Bit Field Set Unbanked (BFSU) or Bit Field Clear Unbanked (BFCU) SPI opcodes. Similarly, when the PSP interface is being used, CRYPTEN cannot be changed by writing to the EIRSET or EIRCLR registers.

Work around

Set or clear the CRYPTEN bit using the Write Control Register (WCR) or Write Control Register Unbanked (WCRU) SPI opcodes, or a direct PSP write to the EIR register.

If the application is not constrained by power consumption, it is possible to set the CRYPTEN bit at device initialization and leave it set.

If the application must change CRYPTEN at run time, care must be taken to ensure that no required interrupt flag bits in EIR are corrupted in the process. For example, if the Link Change Interrupt Flag, LINKIF (EIR<11>), is used by the software, writing to EIR will cause potential loss of information. This can be avoided by sampling the interrupt source (PHYLNK bit in ESTAT) before and after changing CRYPTEN. If the PHYLNK bit has changed, the LINKIF bit can be manually set through a safe BFS operation or write to EIRSET. Any intermediate spurious interrupts on the $\overline{\text{INT}}$ pin can be suppressed by appropriately controlling the EIE interrupt enable bits.

Ideally, if using the SPI interface or using a PSP interface with byte write capability, write only to EIRH and avoid writing to EIRL.

Affected Silicon Revisions

A2							
X							

5. Module: AES

At room temperature, the AES module may compute valid results. However, across voltage, temperature, and ordinary part-to-part device variation, the AES engine will compute incorrect results or fail to finish computations.

Work around

Use a software implementation of AES. For applications based on Microchip PIC® microcontrollers or dsPIC® digital signal controllers, consider using the libraries documented in the Microchip Application Notes *AN953*, "*Data Encryption Routines for the PIC18"* or *AN1044*, "*Data Encryption Routines for PIC24 and dsPIC® Devices"*. The source code for these libraries is available on the Data Encryption Libraries CD, Microchip part number SW300052.

Affected Silicon Revisions

A2							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39935**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

No issues.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2009)

Initial release of this document; issued for revision A2. Includes silicon issues 1 (PHY – Receive), 2-3 (PHY – Transmit), 4 (Memory – SFR) and 5 (AES).

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