

## Transistors

## 2.5V Drive Nch+Nch MOS FET

## UM6K1N

## ●Structure

Silicon N-channel MOS FET


## ●Features

- 1) Two 2SK3018 transistors in a single UMT package.
- 2) The MOS FET elements are independent, eliminating mutual interference.
- 3) Mounting cost and area can be cut in half.
- 4) Low On-resistance.
- 5) Low voltage drive (2.5V drive) makes this device ideal for portable equipment.

## ●Applications

Interfacing, switching (30V, 100mA)

## ●Packaging specifications

Type	Package	Taping
	Code	TN
	Basic ordering unit (pieces)	3000
UM6K1N		

## ●Absolute maximum ratings (Ta=25°C)

&lt;It is the same ratings for Tr1 and Tr2.&gt;

Parameter	Symbol	Limits	Unit	
Drain-source voltage	$V_{DSS}$	30	V	
Gate-source voltage	$V_{GSS}$	$\pm 20$	V	
Drain current	Continuous	$I_D$	$\pm 100$	mA
	Pulsed	$I_{DP}^{*1}$	$\pm 400$	mA
Total power dissipation	$P_D^{*2}$	150	mW	
Channel temperature	$T_{ch}$	150	°C	
Range of storage temperature	$T_{stg}$	-55 to +150	°C	

\*1  $P_w \leq 10\mu s$ , Duty cycle  $\leq 1\%$ 

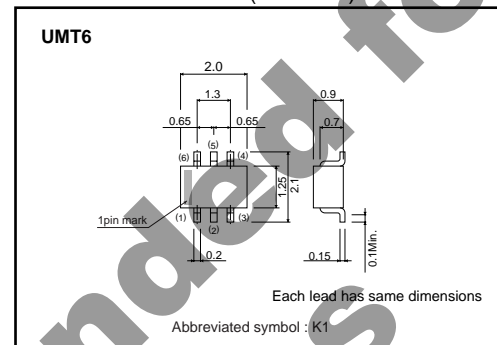
\*2 With each pin mounted on the recommended lands.

## ●Thermal resistance

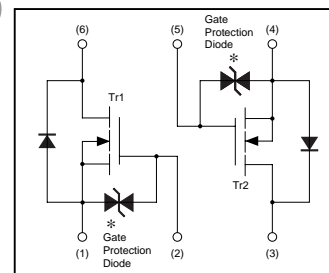
Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}^{*}$	833	°C / W / TOTAL
		1042	°C / W / ELEMENT

\* With each pin mounted on the recommended lands.

## ●External dimensions (Unit : mm)



## ●Inner circuit



- (1) Tr1 Source  
 (2) Tr1 Gate  
 (3) Tr2 Drain  
 (4) Tr2 Source  
 (5) Tr2 Gate  
 (6) Tr1 Drain

\* A protection diode has been built in between the gate and the source to protect against static electricity when the product is in use. Use the protection circuit when rated voltages are exceeded.

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●Electrical characteristics (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	$I_{GSS}$	-	-	$\pm 1$	$\mu A$	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$I_D=10\mu A, V_{GS}=0V$
Zero gate voltage drain current	$I_{DSS}$	-	-	1.0	$\mu A$	$V_{DS}=30V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	0.8	-	1.5	V	$V_{DS}=3V, I_D=100\mu A$
Static drain-source on-state resistance	$R_{DS(on)}$	-	5	8	$\Omega$	$I_D=10mA, V_{GS}=4V$
		-	7	13	$\Omega$	$I_D=1mA, V_{GS}=2.5V$
Forward transfer admittance	$ Y_{fs} $	20	-	-	mS	$I_D=10mA, V_{DS}=3V$
Input capacitance	$C_{iss}$	-	13	-	pF	$V_{DS}=5V$
Output capacitance	$C_{oss}$	-	9	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	$C_{rss}$	-	4	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	$V_{DD}=5V$
Rise time	$t_r$	-	35	-	ns	$I_D=10mA$
Turn-off delay time	$t_{d(off)}$	-	80	-	ns	$V_{GS}=5V$
Fall time	$t_f$	-	80	-	ns	$R_L=500\Omega$ $R_G=10\Omega$

●Electrical characteristic curves

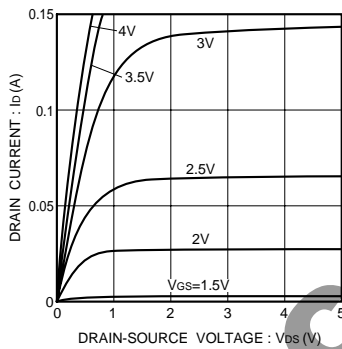


Fig.1 Typical Output Characteristics

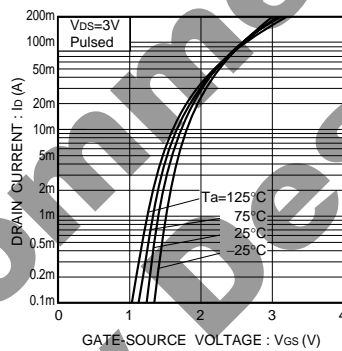


Fig.2 Typical Transfer Characteristics

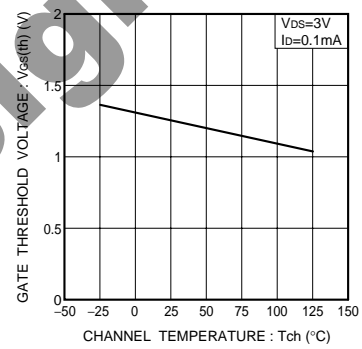


Fig.3 Gate Threshold Voltage vs. Channel Temperature

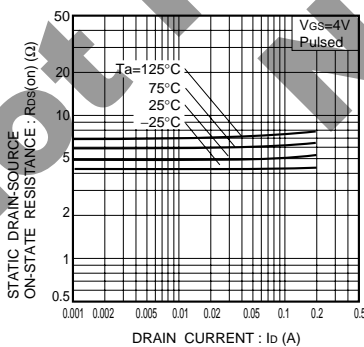


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (I)

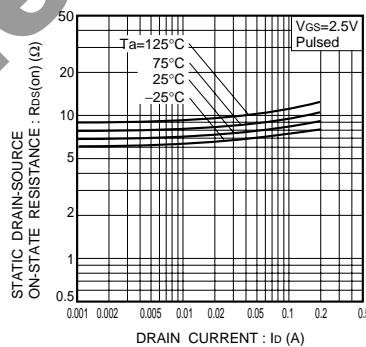


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (II)

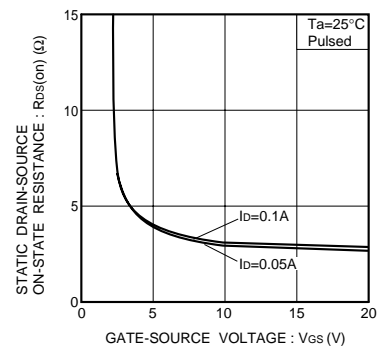


Fig.6 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

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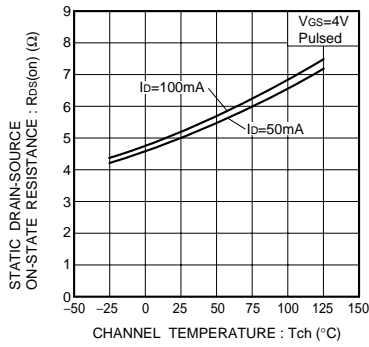


Fig.7 Static Drain-Source On-State Resistance vs. Channel Temperature

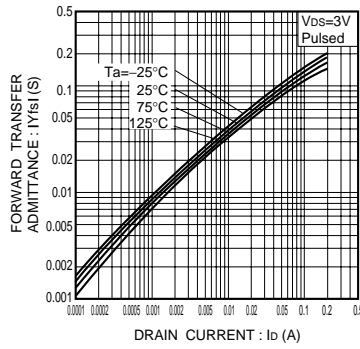


Fig.8 Forward Transfer Admittance vs. Drain Current

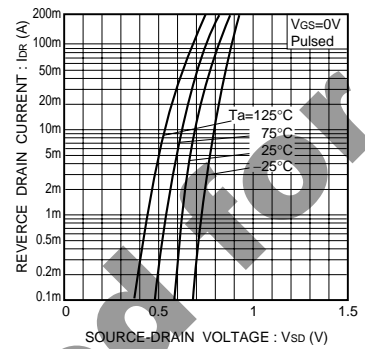


Fig.9 Reverse Drain Current vs. Source-Drain Voltage (I)

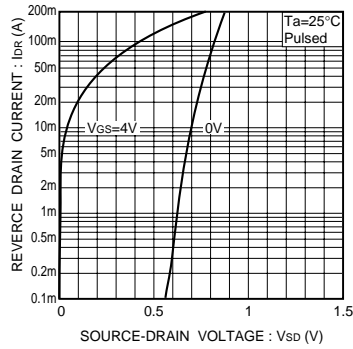


Fig.10 Reverse Drain Current vs. Source-Drain Voltage (II)

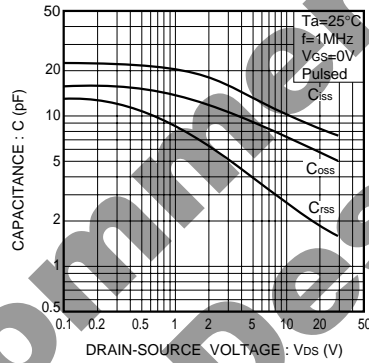


Fig.11 Typical Capacitance vs. Drain-Source Voltage

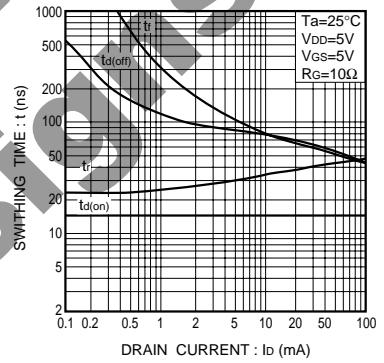


Fig.12 Switching Characteristics

●Switching characteristics measurement circuit

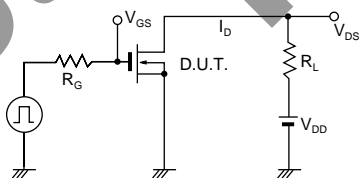


Fig.13 Switching Time Test Circuit

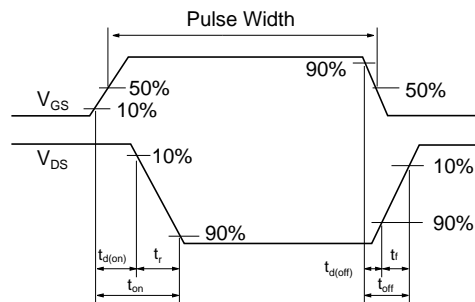


Fig.14 Switching Time Waveforms

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