

## Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use <http://www.nexperia.com>

Instead of [sales.addresses@www.nxp.com](mailto:sales.addresses@www.nxp.com) or [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com), use [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com) (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

# 74AHC377; 74AHCT377

Octal D-type flip-flop with data enable; positive-edge trigger

Rev. 02 — 12 June 2008

Product data sheet

## 1. General description

The 74AHC377; 74AHCT377 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC377; 74AHCT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. A common clock input (CP) loads all flip-flops simultaneously when the data enable input ( $\bar{E}$ ) is LOW. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop. The  $\bar{E}$  input is only required to be stable one set-up time prior to the LOW-to-HIGH transition for predictable operation.

For versions associated with the 74AHC377; 74AHCT377, refer to the following:

- For the master reset version, see 74AHC273; 74AHCT273
- For the transparent latch version, see 74AHC373; 74AHCT373
- For the 3-state version, see 74AHC374; 74AHCT374

## 2. Features

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than  $V_{CC}$
- Ideal for addressable register applications
- Data enable for address and data synchronization
- Eight positive-edge triggered D-type flip-flops
- Input levels:
  - ◆ For 74AHC377: CMOS level
  - ◆ For 74AHCT377: TTL level
- ESD protection:
  - ◆ HBM EIA/JESD22-A114E exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V
  - ◆ CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<b>74AHC377</b>				
74AHC377D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHC377PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
<b>74AHCT377</b>				
74AHCT377D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHCT377PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

### 4. Functional diagram

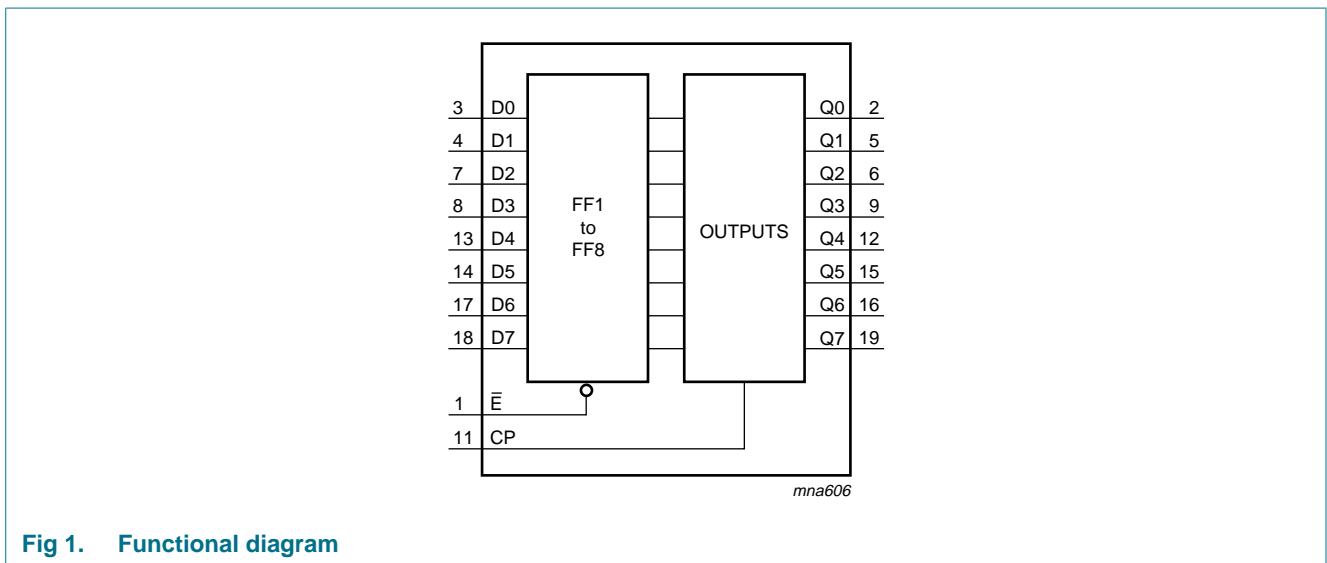


Fig 1. Functional diagram

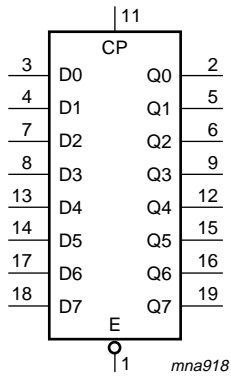


Fig 2. Logic symbol

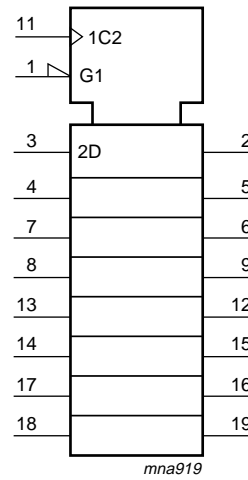


Fig 3. IEC logic symbol

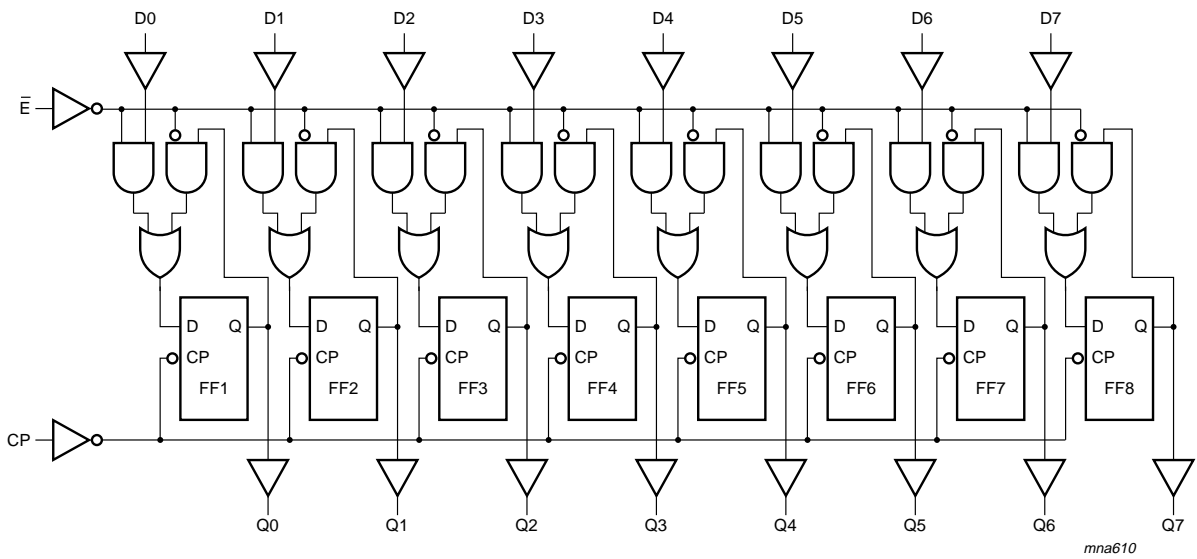


Fig 4. Logic diagram

## 5. Pinning information

### 5.1 Pinning

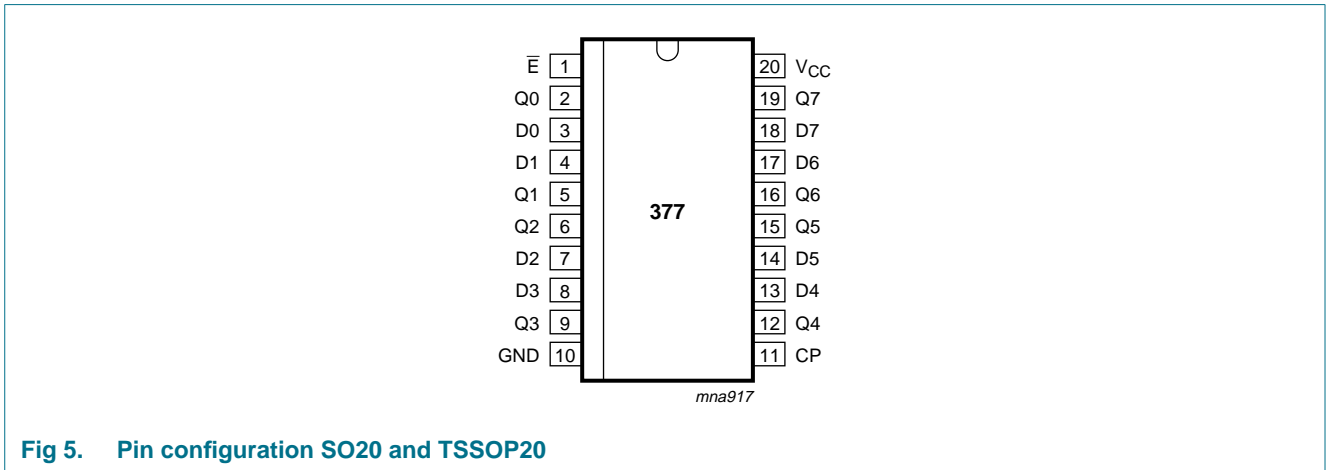


Fig 5. Pin configuration SO20 and TSSOP20

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\bar{E}$	1	data enable input (active LOW)
Q0	2	flip-flop output
D0	3	data input
D1	4	data input
Q1	5	flip-flop output
Q2	6	flip-flop output
D2	7	data input
D3	8	data input
Q3	9	flip-flop output
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge triggered)
Q4	12	flip-flop output
D4	13	data input
D5	14	data input
Q5	15	flip-flop output
Q6	16	flip-flop output
D6	17	data input
D7	18	data input
Q7	19	flip-flop output
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating mode	Control		Input	Output
	$\bar{E}$	CP	Dn	Qn
Load 1	l	↑	h	H
Load 0	l	↑	l	L
Hold (do nothing)	h	↑	X	no change
	H	X	X	no change

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 ↑ = LOW-to-HIGH CP transition;  
 X = don't care.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	<sup>[1]</sup> -20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	<sup>[1]</sup> -20	+20	mA
$I_O$	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5)$ V	-25	+25	mA
$I_{CC}$	supply current		-	+75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	<sup>[2]</sup> -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] For SO20 packages: above 70 °C the value of  $P_{tot}$  derates linearly at 8 mW/K.  
 For TSSOP20 packages: above 60 °C the value of  $P_{tot}$  derates linearly at 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>74AHC377</b>						
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	100	ns/V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	20	ns/V
<b>74AHCT377</b>						
V <sub>CC</sub>	supply voltage		4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC377</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	$\mu\text{A}$
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
<b>74AHCT377</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = -50 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = 50 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; other pins at $V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF



10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max		
<b>74AHC377</b>											
t <sub>pd</sub>	propagation delay	CP to Qn; see Figure 6 <sup>[2]</sup>									
		V <sub>CC</sub> = 3.0 V to 3.6 V									
		C <sub>L</sub> = 15 pF	-	5.6	12.8	1.0	15.0	1.0	16.0	ns	
		C <sub>L</sub> = 50 pF	-	8.0	16.0	1.0	18.0	1.0	20.0	ns	
		V <sub>CC</sub> = 4.5 V to 5.5 V									
		C <sub>L</sub> = 15 pF	-	3.9	9.0	1.0	10.5	1.0	11.5	ns	
f <sub>max</sub>	maximum frequency	see Figure 6									
		V <sub>CC</sub> = 3.0 V to 3.6 V									
		C <sub>L</sub> = 15 pF	80	125	-	70	-	70	-	MHz	
		C <sub>L</sub> = 50 pF	50	75	-	45	-	45	-	MHz	
		V <sub>CC</sub> = 4.5 V to 5.5 V									
		C <sub>L</sub> = 15 pF	125	175	-	110	-	110	-	MHz	
t <sub>w</sub>	pulse width	CP HIGH or LOW; see Figure 6									
		V <sub>CC</sub> = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns	
		V <sub>CC</sub> = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns	
t <sub>su</sub>	set-up time	Dn, $\bar{E}$ to CP; see Figure 7									
		V <sub>CC</sub> = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns	
		V <sub>CC</sub> = 4.5 V to 5.5 V	4.5	-	-	4.5	-	4.5	-	ns	
t <sub>h</sub>	hold time	Dn, $\bar{E}$ to CP; see Figure 7									
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.5	-	-	1.5	-	1.5	-	ns	
		V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	ns	
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[3]</sup>	-	20	-	-	-	-	-	pF	

**Table 7. Dynamic characteristics ...continued**

*Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
<b>74AHCT377; V<sub>CC</sub> = 4.5 V to 5.5 V</b>										
t <sub>pd</sub>	propagation delay	CP to Qn; see <a href="#">Figure 6</a>								
		C <sub>L</sub> = 15 pF	-	4.0	9.0	1.0	10.5	1.0	11.5	ns
		C <sub>L</sub> = 50 pF	-	5.7	10.5	1.0	12.0	1.0	13.5	ns
f <sub>max</sub>	maximum frequency	see <a href="#">Figure 6</a>								
		C <sub>L</sub> = 15 pF	90	140	-	80	-	80	-	MHz
		C <sub>L</sub> = 50 pF	85	130	-	75	-	75	-	MHz
t <sub>W</sub>	pulse width	CP HIGH or LOW; see <a href="#">Figure 6</a>	5.0	-	-	5.0	-	5.0	-	ns
t <sub>su</sub>	set-up time	Dn, $\bar{E}$ to CP; see <a href="#">Figure 7</a>	4.5	-	-	4.5	-	4.5	-	ns
t <sub>h</sub>	hold time	Dn, $\bar{E}$ to CP; see <a href="#">Figure 7</a>	2.0	-	-	2.0	-	2.0	-	ns
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub>	-	23	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V and V<sub>CC</sub> = 5.0 V).

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

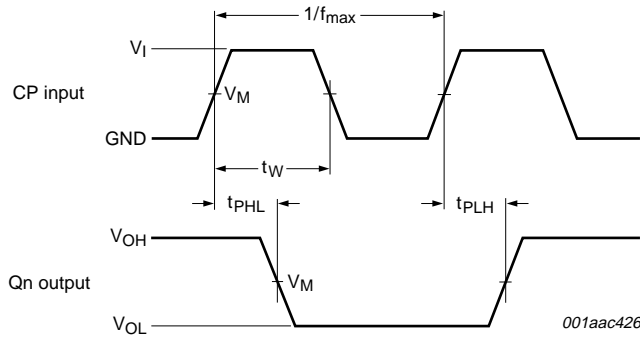
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

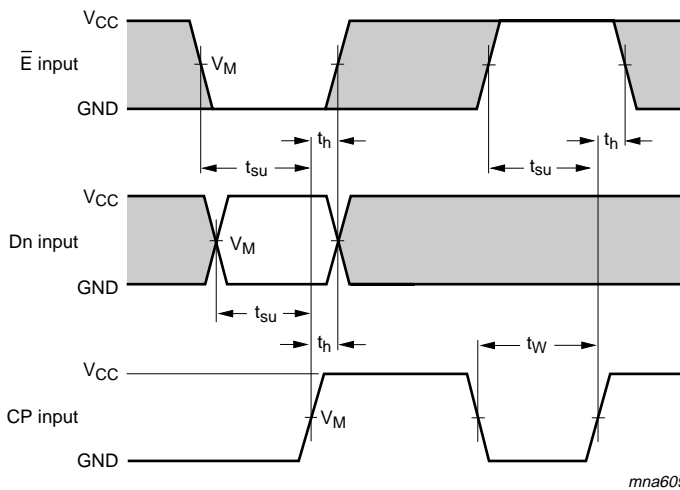
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

## 11. Waveforms



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. Clock pulse width, maximum frequency and input to output propagation delays**

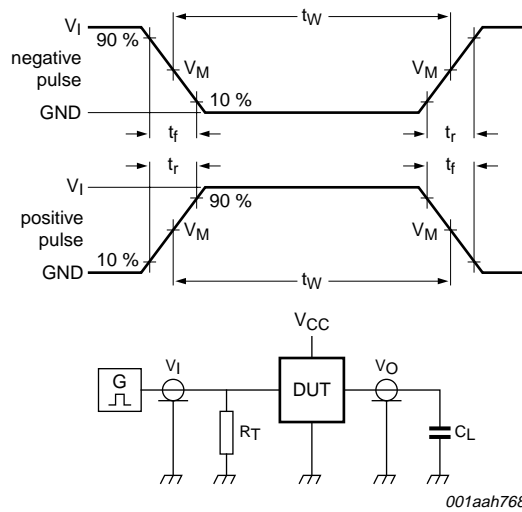


Measurement points are given in [Table 8](#).  
 The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 7. Data set-up and hold times**

**Table 8. Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74AHC377	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT377	1.5 V	$0.5 \times V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

**Fig 8. Load circuitry for measuring switching times**

**Table 9. Test data**

Type	Input		Load	Test
	$V_I$	$t_r, t_f$	$C_L$	
74AHC377	$V_{CC}$	$\leq 3.0$ ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74AHCT377	3.0 V	$\leq 3.0$ ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

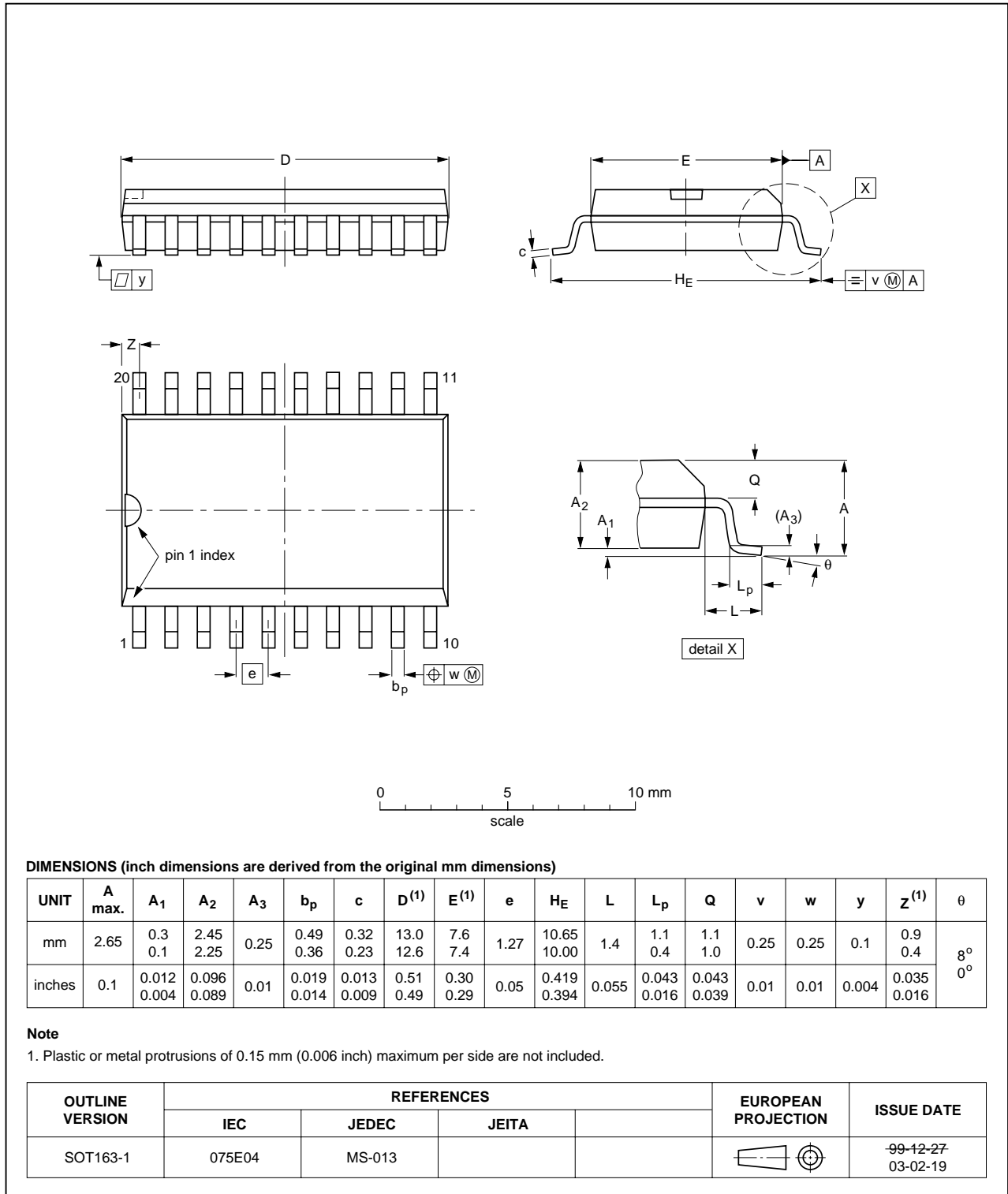


Fig 9. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig 10. Package outline SOT360-1 (TSSOP20)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT377_2	20080612	Product data sheet	-	74AHC_AHCT377_1
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Table 6</a>: the conditions for input leakage current have been changed.</li> </ul>			
74AHC_AHCT377_1	20000815	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 15.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)



## 17. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>4</b>
5.1	Pinning .....	4
5.2	Pin description .....	4
<b>6</b>	<b>Functional description</b> .....	<b>5</b>
<b>7</b>	<b>Limiting values</b> .....	<b>5</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>6</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>6</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>8</b>
<b>11</b>	<b>Waveforms</b> .....	<b>10</b>
<b>12</b>	<b>Package outline</b> .....	<b>12</b>
<b>13</b>	<b>Abbreviations</b> .....	<b>14</b>
<b>14</b>	<b>Revision history</b> .....	<b>14</b>
<b>15</b>	<b>Legal information</b> .....	<b>15</b>
15.1	Data sheet status .....	15
15.2	Definitions .....	15
15.3	Disclaimers .....	15
15.4	Trademarks .....	15
<b>16</b>	<b>Contact information</b> .....	<b>15</b>
<b>17</b>	<b>Contents</b> .....	<b>16</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2008.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 12 June 2008

Document identifier: 74AHC\_AHCT377\_2