



Device Overview

The 89HPES12T3G2, a 12-lane 3-port Gen2 PCI Express® switch, is a member of IDT's PRECISE™ family of PCI Express switching solutions. The PES12T3G2 is a peripheral chip that performs PCI Express Base switching with a feature set optimized for high-performance applications such as servers and storage systems. It provides connectivity and switching functions between a PCI Express upstream port and two downstream ports or peer-to-peer switching between downstream ports.

Features

- ◆ High Performance PCI Express Switch
 - Twelve 5 Gbps Gen2 PCI Express lanes
 - Three switch ports
 - One x4 upstream port
 - Two x4 downstream ports
 - Low latency cut-through switch architecture
 - Support for Max Payload Size up to 2048 bytes
 - One virtual channel
 - Eight traffic classes
 - PCI Express Base Specification Revision 2.0 compliant

- ◆ Flexible Architecture with Numerous Configuration Options
 - Automatic per port link width negotiation to x4, x2 or x1
 - Automatic lane reversal on all ports
 - Automatic polarity inversion
 - Ability to load device configuration from serial EEPROM
- ◆ Legacy Support
 - PCI compatible INTx emulation
 - Bus locking
- ◆ Highly Integrated Solution
 - Incorporates on-chip internal memory for packet buffering and queueing
 - Integrates twelve 5 Gbps embedded SerDes with 8b/10b encoder/decoder (no separate transceivers needed)
 - Receive equalization (RxEQ)
- ◆ Reliability, Availability, and Serviceability (RAS) Features
 - Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)
 - Supports ECRC and Advanced Error Reporting
 - Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O
 - Compatible with Hot-Plug I/O expanders used on PC motherboards
 - Supports Hot-Swap
- ◆ Power Management

Block Diagram

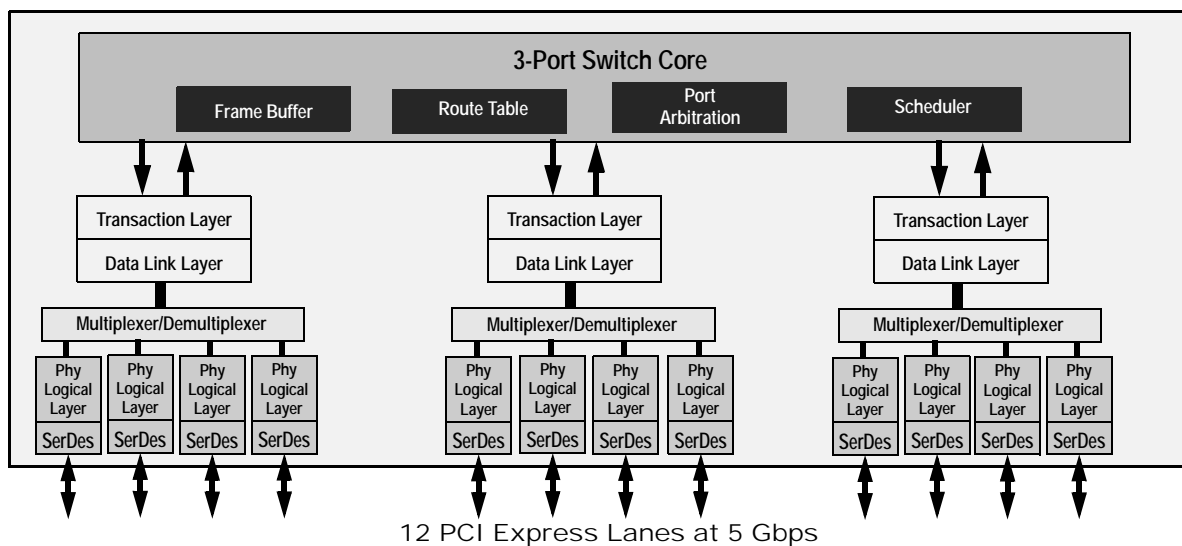


Figure 1 Internal Block Diagram

- Utilizes advanced low-power design techniques to achieve low typical power consumption
- Support PCI Express Power Management Interface specification (PCI-PM 2.0)
- Unused SerDes are disabled.
- Supports Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI) supporting active link state
- ◆ **Testability and Debug Features**
 - Built in Pseudo-Random Bit Stream (PRBS) generator
 - Numerous SerDes test modes
 - Ability to read and write any internal register via the SMBus
 - Ability to bypass link training and force any link into any mode
 - Provides statistics and performance counters
- ◆ **Nine General Purpose Input/Output Pins**
 - Each pin may be individually configured as an input or output
 - Each pin may be individually configured as an interrupt input
 - Some pins have selectable alternate functions
- ◆ **Packaged in a 19mm x 19mm 324-ball BGA with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect the PES12T3G2 provides the most efficient high-performance I/O connectivity device for applications requiring high throughput, low latency and simple board layout. It provides 12 GBps (96 Gbps) of aggregated, full-duplex switching capacity through 12 integrated serial lanes. Each lane provides 5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 2.0.

The PES12T3G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 2.0. The PES12T3G2 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

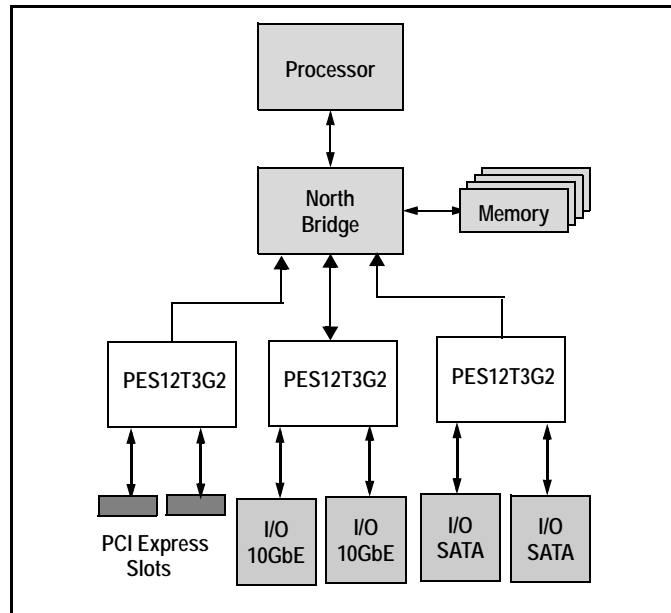


Figure 2 I/O Expansion Application

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